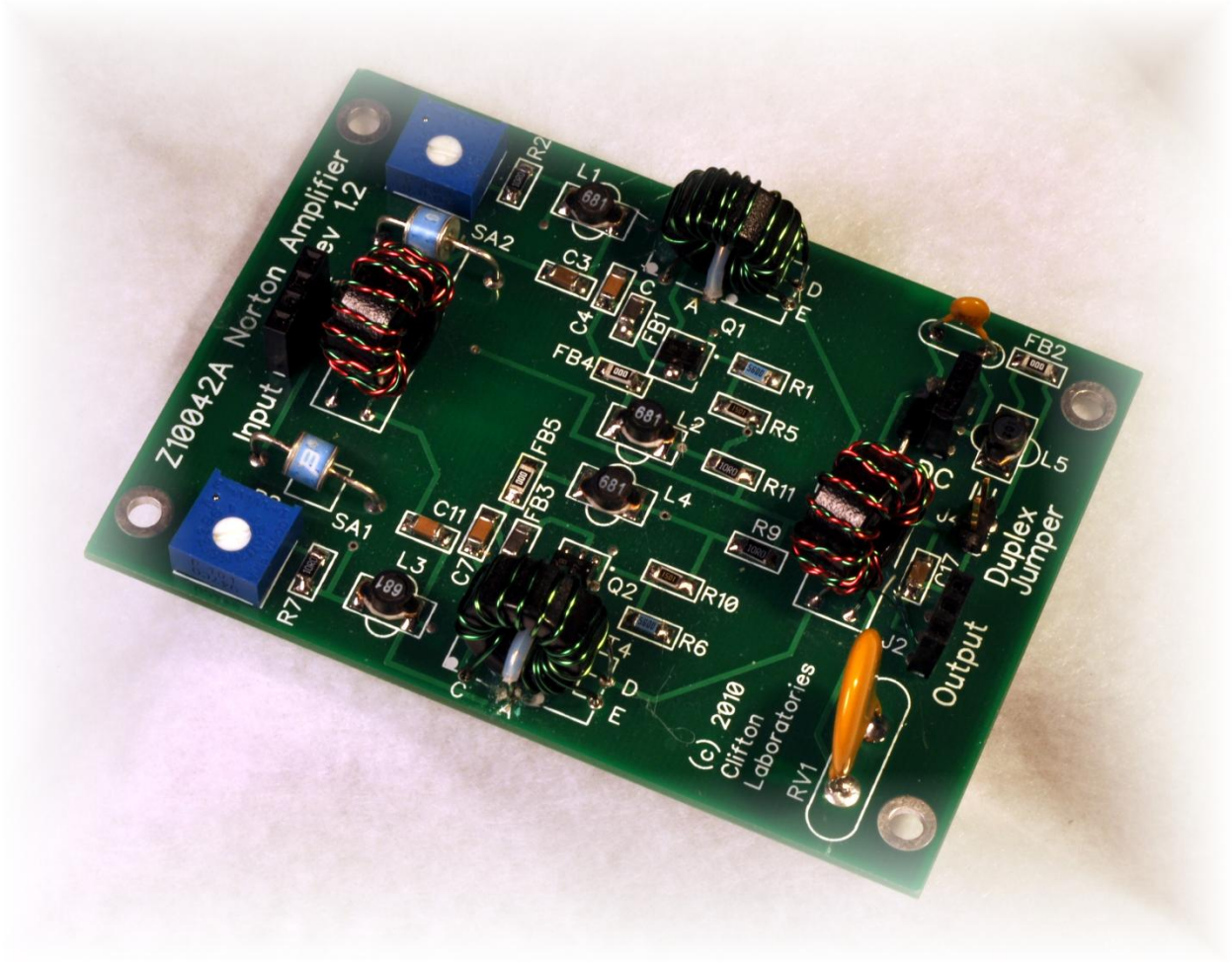
Z10042A
Broadband Norton Amplifier

Assembly and Operation Manual



Revised 11 September 2010

Clifton Laboratories
7236 Clifton Road
Clifton, VA 20124
(703) 830 0368
www.cliftonlaboratories.com

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Applicability of Manual

This manual applies to the Z10042A printed circuit board revision 1.2 and later. The circuit board revision is silk screened on the PCB, just below the model number.



Model Z10042A Broadband Norton Amplifier

Revised 11 September 2010

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Trademarks and Copyright

Material in this document copyrighted © 2010 Clifton Laboratories. All rights reserved. It is provided to allow the Z10042A purchasers to maintain their equipment and such other purposes as may not be prohibited by law.

Warranty

This warranty is effective as of the date of first consumer purchase.

What is covered: During the ninety (90) days after date of purchase, Clifton Laboratories will correct any defects in the Z10042A due to defective parts or workmanship (if purchased as an assembled unit) free of charge (post-paid). You must send the unit at your expense to Clifton Laboratories, but we will pay return shipping. Clifton Laboratories' warranty does not extend to defects caused by your incorrect assembly or use of unauthorized parts or materials or construction practices.

What is not covered: If the Z10042A is purchased as a kit, this warranty does not cover correction of assembly errors or misalignment; repair of damage caused by misuse, negligence, or builder modifications; or any performance malfunctions involving non-Clifton Laboratories accessory equipment. *The use of acid-core solder, water-soluble flux solder, or any corrosive or conductive flux or solvent will void this warranty in its entirety.* Damage to the Z10042A or equipment connected to it caused by lightning strikes is not covered under the warranty. Whether purchased as an assembled unit or as a kit, also not covered is reimbursement for loss of use, inconvenience, customer assembly or alignment time, or cost of unauthorized service.

Limitation of incidental or consequential damages: This warranty does not extend to non-Clifton Laboratories equipment or components used in conjunction with our products. *Any such repair or replacement is the responsibility of the customer. Clifton Laboratories will not be liable for any special, indirect, incidental or consequential damages, including but not limited to any loss of business or profits.*

Under no circumstances is Clifton Laboratories liable for damage to your equipment connected to the Z10042A resulting from use of the Z10042A, whether in accordance with the instructions in this Manual or otherwise.

Safety Information

The Z10042A operates with a user-supplied DC power supply of 13 to 15 Volts at 100 to 120 mA. The Z10042A, although designed as a low signal level preamplifier, is capable of RF output power approaching the 1 watt level. This output power is capable of damaging receivers or the receiver section of a transceiver or test equipment. It is the user's responsibility to ensure that the Z10042A is properly connected to whatever devices it will be used with.

The Z10042A has no replaceable fuses; rather a self-resetting polyfuse limits short circuit current to approximately 200 mA.

The Z10042A is designed to be used only with receive-type power levels. It should not be used with transmitting equipment. The Z10042A's maximum permitted input RF power is 100 mW (+20 dBm). *Power in excess of this level may damage the Z10042A or equipment connected to it, or both. In addition, since the Z10042A has appreciable gain, output power levels sufficient to damage connected equipment may occur with input signal levels well below +20 dBm.*

Although the Z10042A contains protective measures, all of these protection measures assume that the Z10042A is properly grounded and that good engineering practices have been used in its installation and construction of the ground system. The Z10042A is not intended to survive a direct lightning strike to an antenna connected to its input, whether powered up or not. However, the protective measures incorporated into the Z10042A's design should aid in reducing damage.

General Information and Specifications

Description

The term "Norton Amplifiers" refers to a class of transformer feedback amplifiers developed by Dr. David Norton and described in his US Patent No. 3,891,934, granted June 24, 1975 and now in the public domain. (A copy of Dr. Norton's patent is Appendix C to this Manual.) A Norton amplifier permits the distortion reducing benefits of negative feedback to be applied without impairing the amplifier's noise figure. Hence, Norton amplifiers are also known as "noiseless feedback" amplifiers.

The Z10042A is a broadband (50 KHz to 30 MHz) Norton-style amplifier providing 11 dB gain (other gain values are possible) with very high 3rd order and 2nd order intermodulation intercepts, IP3 and IP2, respectively, with a noise figure well below 2 dB over the range 10-30 MHz. The Z10042A is designed for either indoor or outdoor use, with DC power supplied through either separate connections or duplexed over the output coaxial cable. Optional indoor and outdoor die cast enclosures are available for the Z10042A.

The Z10042A is derived from the Norton Amplifier developed by Dr. Dallas Lankford and described in his publication *Common Base Transformer Feedback Norton Amplifiers*, dated 8 June 1994, revised 21 May 2007, available at http://www.kongsfjord.no/dl/Amplifiers/Common%20Base%20Transformer%20Feedback%20Norton%20Amplifiers.pdf.

The Z10042A modifies Dr. Lankford's design in several respects:

- Automatic input disconnect upon DC power removal along with over-voltage gas trap protection
- Improved performance below 500 KHz.
- Over voltage and reverse voltage protection on the DC Power.
- DC power either separately or duplex power.
- Optional balanced or unbalanced input.
- Shunt fed to reduce effect of DC saturation of T2 and T4

Clifton Laboratories also offers the Z1203A DC power injector usable with the Z10042A to provide DC power over the output coaxial cable. This is useful for remote mounted amplifiers.

The Z10042A is available as a kit, including a double sided, silk screened solder masked printed circuit boards and all electronic parts or as an assembled and tested printed circuit board. Options include an indoor enclosure with BNC connectors or an outdoor weatherproof die cast enclosure with a choice of BNC, UHF or Type N connectors.

Typical kit construction time is three to five hours depending on your work practices. The kit is suitable for relatively inexperienced builders, although Clifton Laboratories does not recommend it to purchasers who have never built an electronic kit before. Also, if you have never wound a toroid inductor or transformer, you might wish to ask an experienced builder to show you how it's done.

Specifications

Parameter	Value
PCB Dimensions	3.50” x 2.50” x 0.75” vertical clearance required. (88.9mm x 63.5mm x 19mm). Four mounting holes for 4-40 screws provided, template in Appendix B.
DC Power Required	Maximum: 15V Minimum: 13.8V [may not meet specifications below this voltage. See Appendix D for performance versus supply voltage considerations.] Negative to ground, typical DC current 60-100 mA depending on bias adjustment. As an option, a reduced power version of the Z10042A is available, with approximately 25 mA, usable down to 12V input. 2nd and 3rd order intermodulation performance is degraded with this option; noise figure is improved over normal idle current.
Maximum RF Power Input	Do not exceed 100 milliwatts (+20 dBm). IP3 performance specifications are based upon -10 dBm signal input; performance not warranted at greater input levels.
Test Conditions	Performance data is for a 1:11:4 turns ratio design, 13.8 VDC after adjusting balance trimpots for minimum 2nd harmonic distortion. Unless otherwise indicated, performance measurements are made with direct DC power, not duplexed. Figures stated as “typical” are not warranted.
3 dB Bandwidth	100 KHz – 30 MHz. Typical -3 dB bandwidth 50 KHz - 45 MHz
2nd and 3rd Order Intermodulation Intercept	Measured with 3 and 4 MHz input tones, adjusted for 0 dBm output from the Z10042A. Protocol as discussed later in this manual. Intercepts are output referenced. OIP2: +80 dBm (typically > +90 dBm) OIP3: +45 dBm (typically +46 to +48 dBm)
Gain	11 dB nominal at 1 MHz.
1 dB Gain Compression	+19 dBm input.
Noise Figure	2.0 dB maximum 10-30 MHz. Typically 1.5 dB 10-30 MHz.
Input VSWR	When terminated with 50 ohm load, input VSWR is less than 2:1 over the range 300 KHz – 30 MHz, and is typically below 1.5:1 over this range.
Common Mode Rejection in Balanced Input Mode	Typically 50 dB at 1 MHz, decreases with increasing frequency.

Assembly

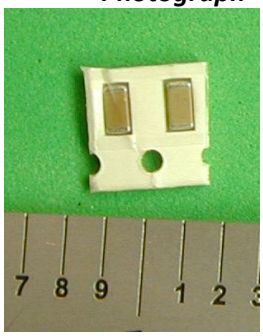
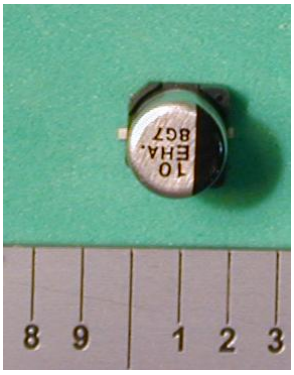
Parts Provided

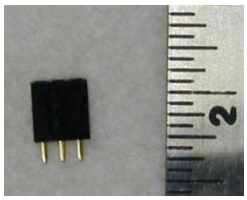
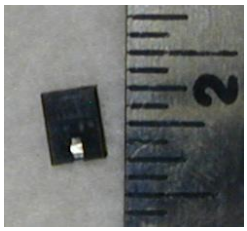
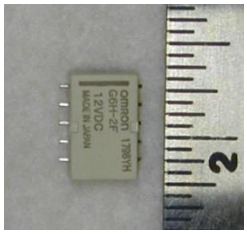
Before starting your build, please take a moment and inventory the parts provided against the list below. The ruler is marked in decimal (tenths) inches. One inch is 25.4mm and 0.1 inch is 2.54mm. (Some older photos use a ruler marked in fractions of an inch, such as 1/16th.)

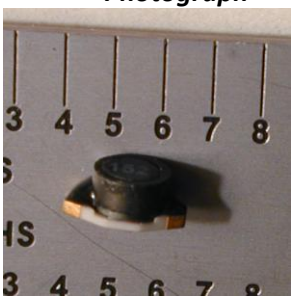
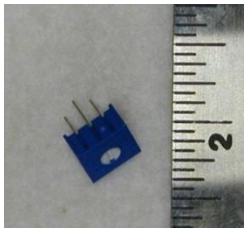
⚠ Many parts in this kit are not marked and can easily be confused. Parts are provided in individually labeled paper envelopes. Please keep parts in the associated envelope when not being installed.

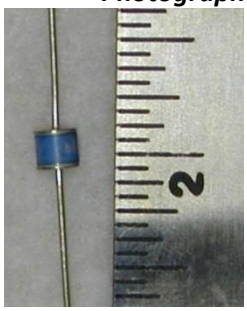
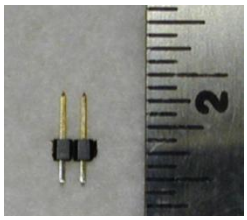
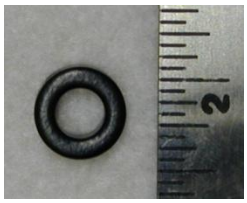
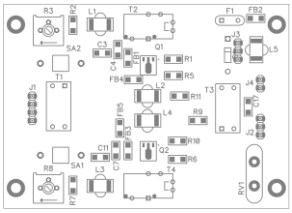
A note on how component values are identified in this manual

This document follows the international practice of using the value multiplier to indicate the decimal point. Thus, a 1.0µF capacitor is identified as 1µ0 and a 10,000 ohm resistor is identified as 10K0.

Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	12	C2, C3, C4, C6, C7,C10, C11, C14, C15, C16, C17, C18,	1uF X7R 25V, 1206 size surface mount ceramic capacitors.	None
Same as above	4	C20,C21,C22, C23	10pF, C0G 50V, 1206 size surface mount ceramic capacitors	None
Same as above	2	C5, C8	1000pF, C0G 50V, 1206 size surface mount ceramic capacitors	None
	1	C19	10uF/25V 105°C aluminum electrolytic capacitor.	10 EHA

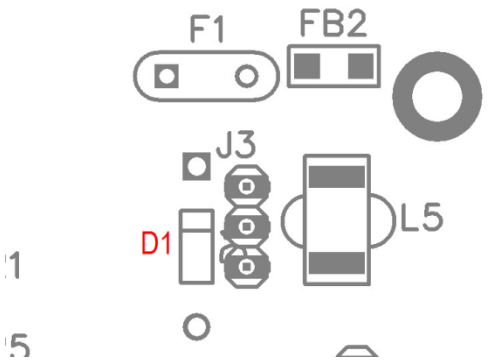
Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	1	D1	Silicon diode, 1A or greater, 100V or greater. Typically a 1N4007 part	1N400x where X may be any number from 0 to 7
	1	F1	200 mA Raychem “polyfuse” PTC varistor. The supplied part may or may not have a “crimped” lead.	XF020
	2	FB1,FB3	Surface mount ferrite bead	None
	3	FB2, FB4 & FB5	These three components are not used and are replaced with 000 ohm 1206 jumpers	000
	2 [3-place] 1 [4-place]	J1, J2, J3	J1: 4-place J2 & J3: 3 place 0.1 inch header sockets	None
	1	None	Shorting jumper for 2 place 0.1 inch header pins	None
	1	K1	G6H-2F-DC12 double pole, double throw 12V surface mount relay	G6H-2F-12VDC

Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	5	L1, L2, L3, L4 & L5	1m0 RF choke (shielded) high current	102
	2	Q1, Q2	NPN transistor, UHF, type NE85634, SOT-89 package	RE
	¼ watt, 1% 1206 Surface Mount Resistors			
	2	R1,R6	560R	5600
	2	R4,R12	49R9	49R9
	2	R10, R5	1K50	1501
	4	R2, R7, R9,R11	10R0	10R0
	2	R3, R8	100R Trim-pot	101
	1	RV1	14mm dia. 18V over-voltage MOV	180M

Photograph	*Qty*	*ID*	*Description and Comments*	*Component Marking*
	2	SA1, SA2	Spark gap Either of the following may be provided: 90V 75V	90V (and date code) EC 75 (and date code)
	12	J4	Total of 12 pins supplied. 2 pins for J4; remaining pins for input/output wiring. Pins are 0.1 inch spaced, 0.025 inch square gold flashed.	None None
	4	T1,T2,T3, T4	0.5 inch diameter ferrite cores; builder to wind. **NOTE: DIFFERENT CORE MATERIALS ARE USED FOR T1/T3 AND T2/T4. THE CORES ARE SEPARATELY PACKAGED. DO NOT INTERCHANGE THE CORES.**	None
	1	PCB	Printed circuit board. Identified as Z10042A	Z10042A and revision number
None	1 length #24 wire	None	No. 24 AWG magnet wire, use for T2 and T4	None
None	2 lengths #26 wire	None	No. 26 AWG magnet wire, use for T1 and T3. One length red, one length green.	None
None	2 inches (50mm) foam tape	None	Length of ¼ inch (6mm) wide, double sided foam tape	None
None	4 inches (100mm)		Teflon insulated solid wire	None

Errata:

D1 outline is on PCB; component ID is obscured by J3.



Overview of Installing Surface Mount Parts

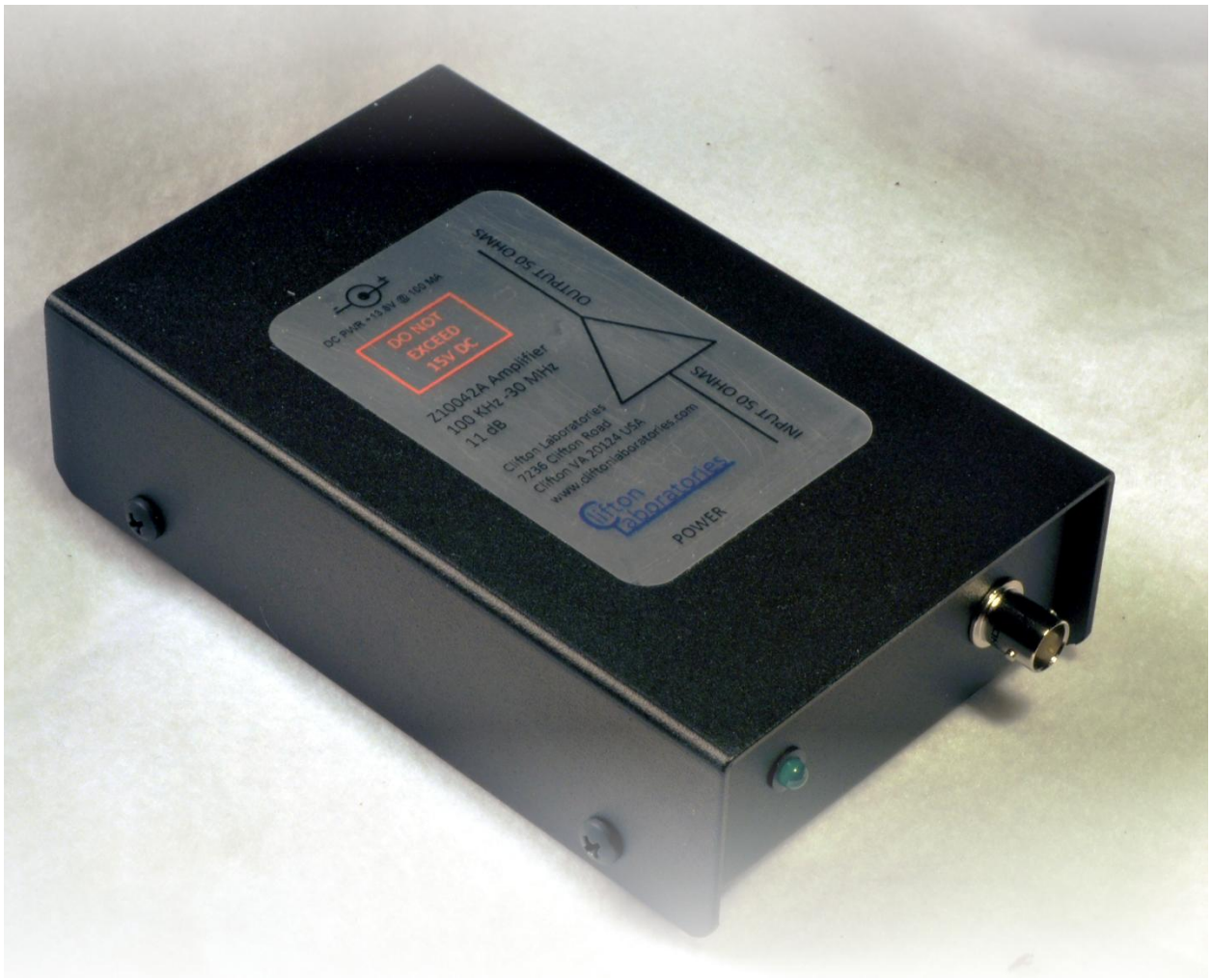
1. If the component has one pad that is a ground, lightly tin the non-ground pad. If neither pad is a ground connection, tin either one of the pads.

2. Using forceps or a very light touch with long nose pliers, slide the component into place while heating the tinned pad. Check that the component is more or less centered on the pads and remove the soldering iron when centered. Too much pressure will crack these parts so use a light touch.

3. Solder the other pad. Touch up the first pad if necessary.

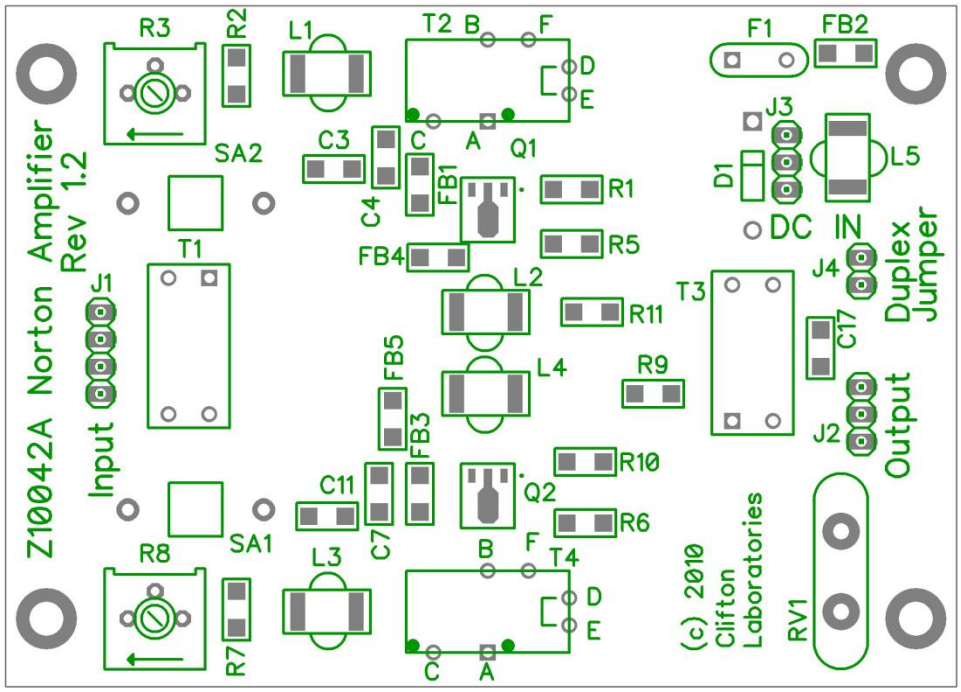
4. Although the Z10042A's ground pads use "thermal relief" it may still be difficult to make with a small soldering pencil, as the large foil area requires more heat capacity than a normal floating pad.

The image below shows a Z10042A installed in the optional enclosure.

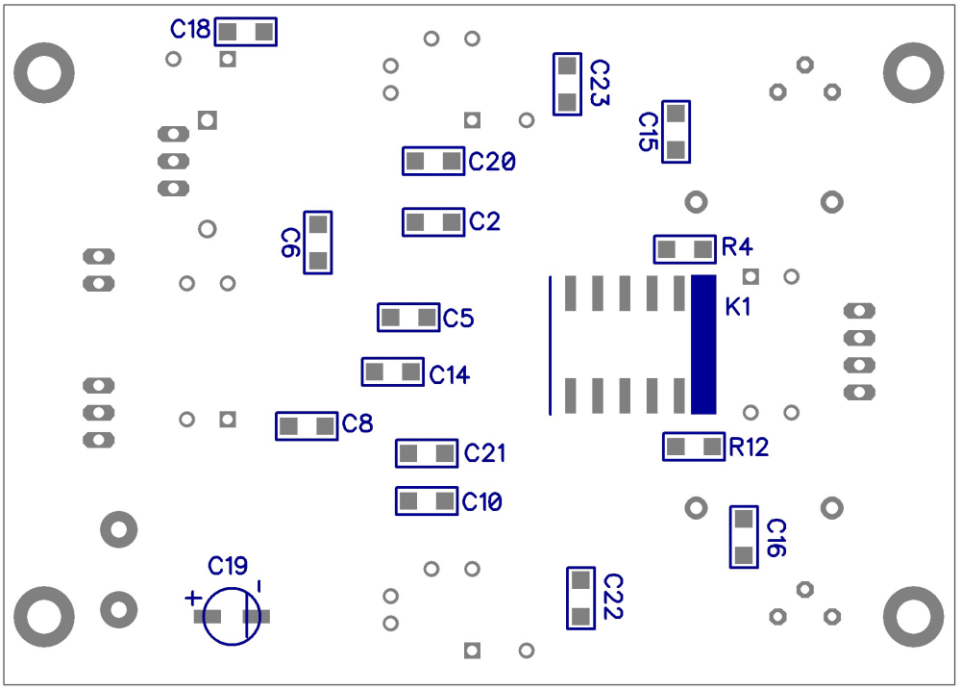


Component Layout

TopV iew



Bottom View



Assembly Order

The Z10042A is a relatively simple kit. The most complex part is winding the transformers, and even this is not difficult.

If available, apply RMA flux from a flux pen, such as Kester 83-1000-0186 to all pads.



The assembly order starts with the bottom surface.

- ❑ Install 1uF capacitors at 7 places:
  C10, C14, C15, C16, C18, C2 & C6

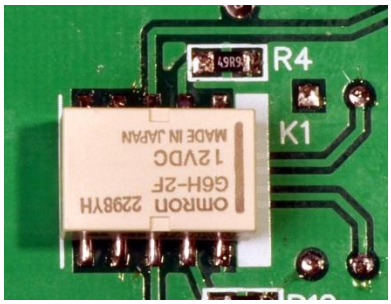
- ❑ Install 10pF capacitors at 4 places:
  C20, C21, C22 & C23

- ❑ Install 1000pF capacitors at 2 places:
  C5, C8

- ❑ Install C19, a 10uF electrolytic capacitor marked 10. <u>This is a polarized part and must be installed with the correct orientation</u>. *Negative is indicated with black stripe on the capacitor body.*

  C19 may be difficult to properly solder as its leads are largely below the base insulator. Before soldering, tin C9's positive lead. Apply a small amount of solder to C9's PCB pad. While heating the positive pad with the soldering iron, hold C19 in place and apply a small amount of pressure with your fingers or forceps. After soldering the positive pad, verify it is properly attached; C19 should not move under light pressure. Then solder the negative terminal.

- ❑ Install K1, a double pole, double throw relay, marked G6H-2F.

  K1 orientation should follow the photograph at the right; the black strip on the relay body is next to the wide white band on K1's PCB outline.

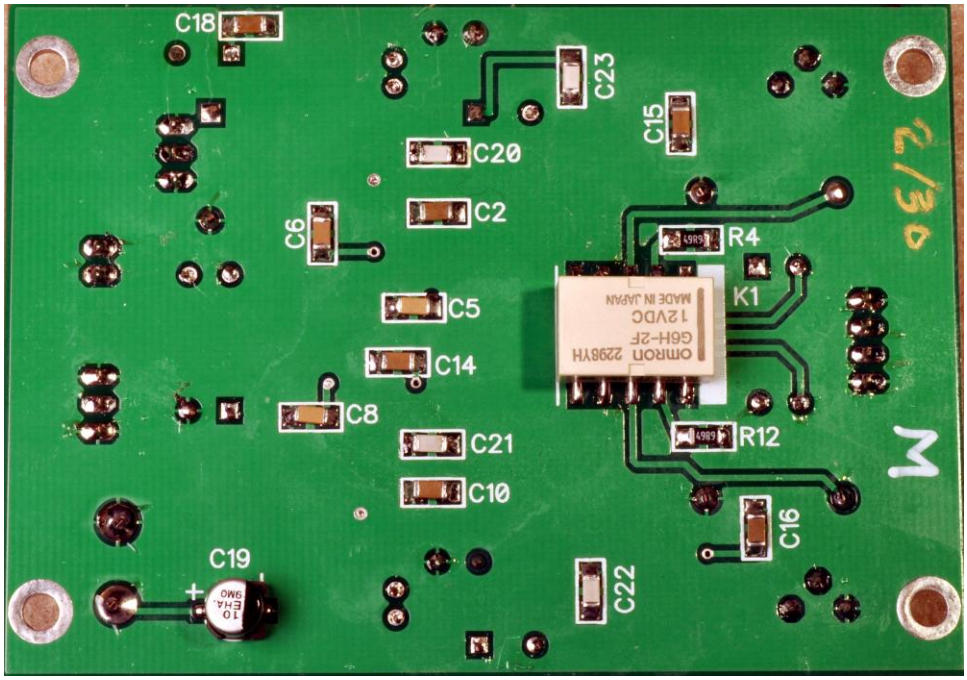
  When soldering K1 in place, tin one corner pad and slide K1 into place whilst keeping the solder molten. Align K1's pins with the pads and remove the soldering iron. Then solder the remaining pins.

- ❑ Install R4 and R12, 49.9 ohm resistors, marked 49R9.

- ❑ This completes the bottom assembly. Check your work for missing parts and poor solder

joints.

The completed bottom surface is shown below.



Top Surface Components

- ❑ Install 1uF capacitors at 5 places:
  C3, C11, C4, C7 & C17

- ❑ Install Q1 and Q2, NE85634 transistors, marked RE.

  To install Q1 and Q2, Apply a small bit of solder to one outside pad. Hold the transistor in place with tweezers and apply heat to the top of the pin, melting the solder on the pad beneath the pin. Solder the remaining two pins in place and reflow the tacked pin. Then solder the collector tab in place.

- ❑ Install 10R0 resistors, marked 10R0, at 4 places:
  R2, R7, R9 & R11

- ❑ Install ferrite beads (unmarked) in 2 places:
  FB1 & FB3.

- ❑ Install zero ohm jumpers (marked 000) in 3 places:
  FB2, FB4 & FB5.

- ❑ Install 560R resistors (marked 5600) in 2 places:
  R1 & R6

- ❑ Install 1K50 resistors (marked 1501) in 2 places:
  R5 & R10

❑ Install 1m0 inductors (marked 102) at 5 places.
L1, L2, L3, L4 & L5

These inductors may be installed one of three ways:

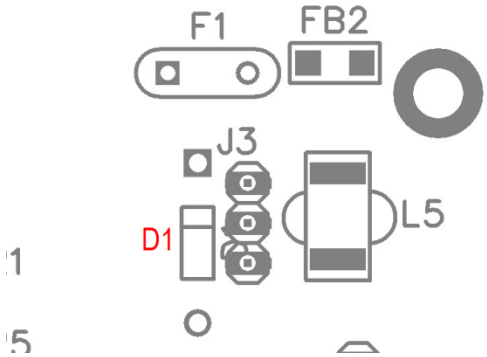
- Clamp the inductor in place with a clamp made from a wooden spring clothespin. Solder one pad and remove the clamp. Solder the remaining pad.
- Position the inductor, centering it on the pads. Carefully apply the soldering iron and solder to one pad. The molten solder should flow around the inductor and hold it in place. Solder the remaining pad.
- Tin one pad. Apply the soldering iron to the tinned pad and slide the inductor in place. When positioned and after the solder has wetted the inductor tab, remove the soldering iron and allow the joint to cool. Then solder the remaining pad.

After building many circuit boards with these inductors, I use the second method. If this is the first time you have installed one of these parts, I recommend the first or third method.

❑ Install D1, the reverse polarity protection diode. This will be a 1N400x series device, marked 1N400x where x may by any digit from 0 to 7.

The silk screen ID for D1 is obscured by J3, so refer to the illustration at the right for D1's location.

Observe polarity when installing the diode; the diode body will be marked with a bar or ring around one end. The lead from the marked end goes into the pad marked with a bar and the + sign.



❑ Install F1 (RXE020 200 mA polyfuse, marked XF020). Depending on the available product, this component may have parallel, crimped leads or angled leads.

To install the crimped lead version, slip one lead into the mounting hole so that the kink or crimp snaps across the PCB. Put the second lead into the other mounting hole and gently pull (with long nose pliers) the second lead from the underside of the board until it likewise snaps into the mounting hole. If this process is too difficult, you may simply install F1 with the crimped leads above the PCB surface. Solder.

If the angled leaded device is provided, install until the bend in the lead contacts the top of the printed circuit board pad. Solder.

❑ Install RV1, the MOV over-voltage protector, marked 180M. RV1 is not polarized and may be installed in either orientation.

❑ Install R3, a 100R trimpot, marked 101.

❑ Install R8, a 100R trimpot, marked 101.

❑ Install the three-pin header socket (female) at J2.

❑ Install SA1 and SA2,spark gaps, marked either 90V plus a date code or EC75 plus a date code. SA1 and SA2 are not polarized and may be installed in either orientation. Be careful when bending the leads as the ceramic body is fragile. SA1 and SA2 should be installed with their body approximately 1/8th inch (3 mm) above the PCB surface.

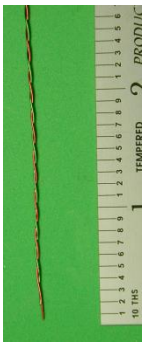
❑ Install the three-pin header sockets (female) at J3

❑ Install the four-pin header sockets (female) at J1

❑ Locate the header pin (male) strip and break or cut two pins from the strip. Install the two pins at J4. (The short side goes into the pad holes.)

At this point, all components should be installed on the PCB's top surface, except for the four transformers.

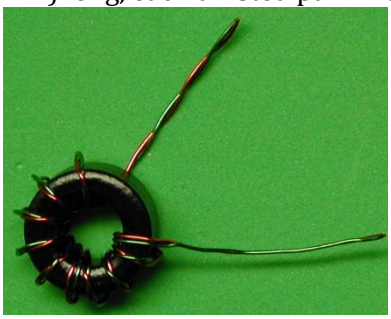
❑ Locate the No. 26 AWG magnet wire. (It is the smaller diameter of the two wire sizes.) One length of green insulated wire is provided and one of red insulated wire.



Cut four lengths of the wire:
Two pieces green, each 11 inches (280 mm) long.
Two pieces red, each 11 inches (280 mm) long.

Take one piece of red wire and one piece of green wire and twist approximately 60 turns. Repeat for the second pair of red and green wires. (A variable speed drill, running slow speed, speeds up the twisting process.)

At this point, you should have two twisted wire sections, each approximately 11 inches (280 mm) long, each twisted pair with one red and one green wire.

❑ 

Wind the twisted wire 10 turns onto one of the ferrite cores <u>marked as to be used for T1 and T3</u>.

As a reminder, a turn is counted when the wire passes through the hole in the core.

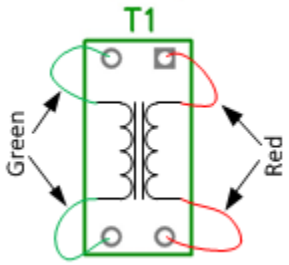
Start by inserting the cut end approximately one inch (25 mm) through the core. Thread the doubled end through and wind 10 turns. Space the turns so that the windings occupy approximately 75% of the core perimeter (270 degrees if you prefer to think in those terms).

Repeat for the second transformer, using a core identified as for T1 and T3.

Congratulations. You have completed winding two bifilar broadband transformers, T1 and

T3.

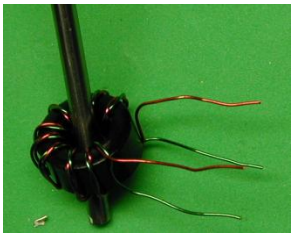
Locate the PCB and look at the silk screen outline for T1 and T3. Note that each has four pads, comprised of three round pads and one square pad, oriented as shown in the drawing.



The green wires connect to the two round pads on one side and the red wires connect to the one square and one round pad on the opposite side. [This is not critical and one can interchange the green and red leads, but troubleshooting will be easier if all the Z10042A's are built the same way.]

Un-twist the pigtails so that you have four separated wires. Remove the insulation and tin the four wires.

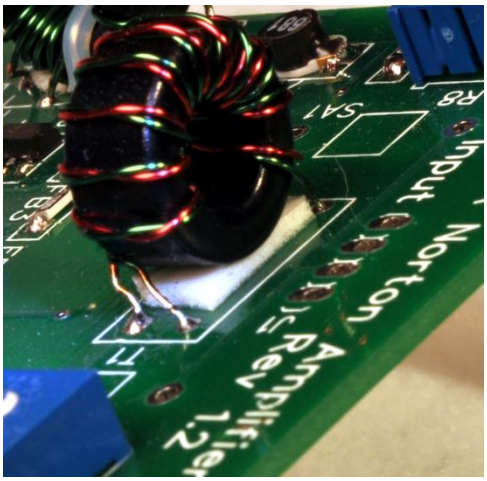
The wire leads should be formed as illustrated in the photo to the right.



Cut a length of foam tape approximately 3/8ths of an inch long (9mm) and apply it to the PCB within the T1 outline. Make sure that tape does not block the pad holes, and trim if necessary.

Install T1 as shown in the drawing.

Note: The red and green wire supplied is "solderable" and the insulation will melt if heated with a blob of molten solder. This heating and tinning must be done <u>before</u> the transformers are installed in the PCB.



A common error in installing T1 and T3 (as well as T2 and T4) is that the insulation is not fully removed from the wire due to insufficient heating.

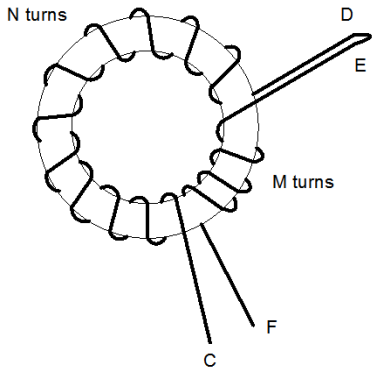
❑ Repeat the process for T3 and install

❑ ⚠ The remaining step is to wind T2 and T4, the matching and feedback transformers. These transformers should be wound as identical as possible and <u>must</u> be phased (wound) as described below or else you will build an oscillator instead of an amplifier. If you <u>carefully</u> follow the instructions in this manual, your transformers will work the first time. Before winding T2 and T4, take a moment to read the installation steps and study the drawing and photographs.

This manual describes transformers resulting in 11 dB nominal gain, with a 1:11:4 winding

ratio. Other winding ratios are possible with different gain as described elsewhere in this manual. In the context of drawing below, this configuration is N=11, M=4.

❑ Cut two lengths of #24 AWG magnet wire, each length 16 inches (400 mm) long.



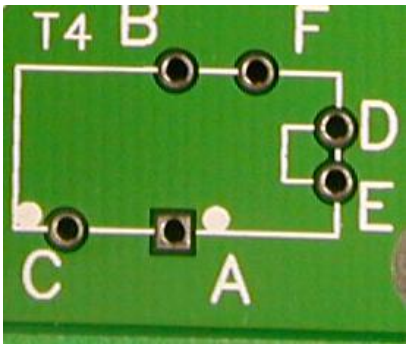
This wire will be wound 15 turns on a ferrite core, as illustrated at the right. The letters C…F on the drawing correspond to T2 and T4's PCB pads. Before winding the transformers, take a moment and look at the PCB outline for T2 and T4.

<u>The cores used should be from the envelope marked for use with T2 and T4.</u>

Start by threading the wire through the core with approximately one inch (25 mm) projecting from the core. This short starting end is C in the drawing.



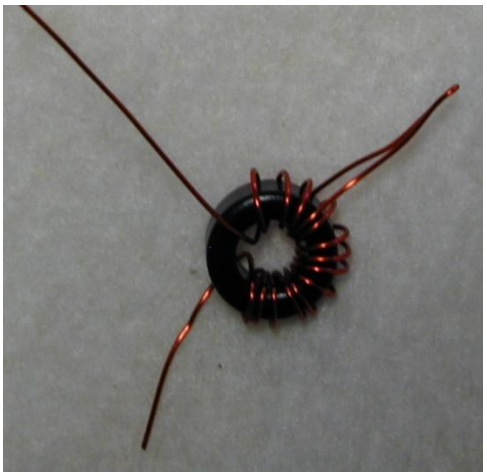
Wind 11 turns (N) <u>following the orientation shown in the drawing. Note the direction of winding.</u> (I'm left handed and this is how I wind a toroid. <u>And, more importantly, the sense of winding A-B, which is defined by the PCB layout, is based upon following the winding direction illustrated in the drawing.</u>) When completed with all 15 turns, the winding will occupy 80 to 85% of the core perimeter.

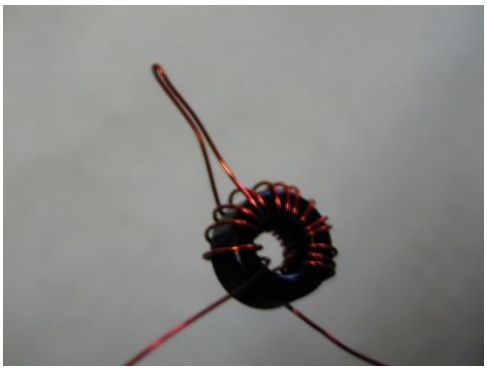


As a reminder, a turn is counted when the wire passes through the hole in the core.

Extend the 11th turn approximately one inch (25 mm) and double it back. (The doubled wire will become ends D and E). Wind four more turns (M), ending at end F. Trim the F wire to be approximately one inch (25 mm) long.

The photos below shows a transformer at this stage, before the loop is cut and the end wires trimmed.





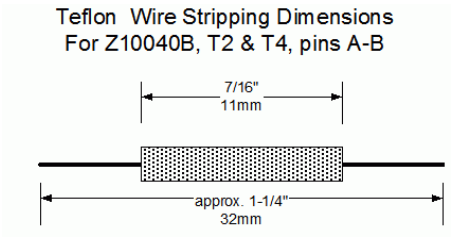
❑

Cut the loop so that the two free ends are approximately one inch (25 mm) long. Remove the insulation on all four ends and tin. You may find it helpful to fit the transformer into the PCB to see how it fits before continuing to the next step.

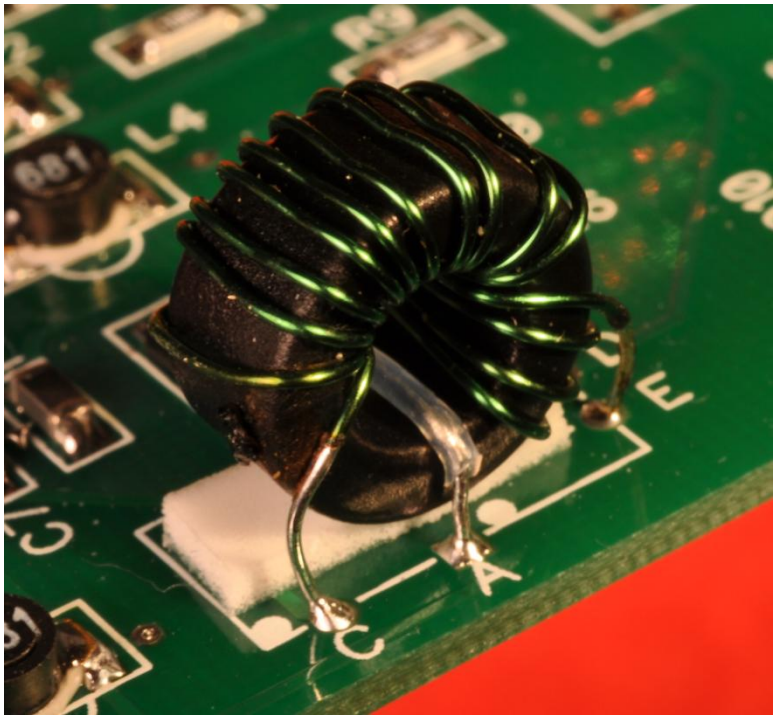
❑ Cut a length of foam tape approximately ½ inch (12mm) long and apply it to the PCB within the within the T2 outline. Make sure that tape does not block the pad holes, and trim if necessary.

Insert the leads into T2 holes C, D, E and F, following the drawing, and solder these four leads.

❑ Locate the short length of Teflon insulated wire and cut it into two lengths and remove the insulation as shown in the drawing. These will be the one turn input winding between pads A and B.



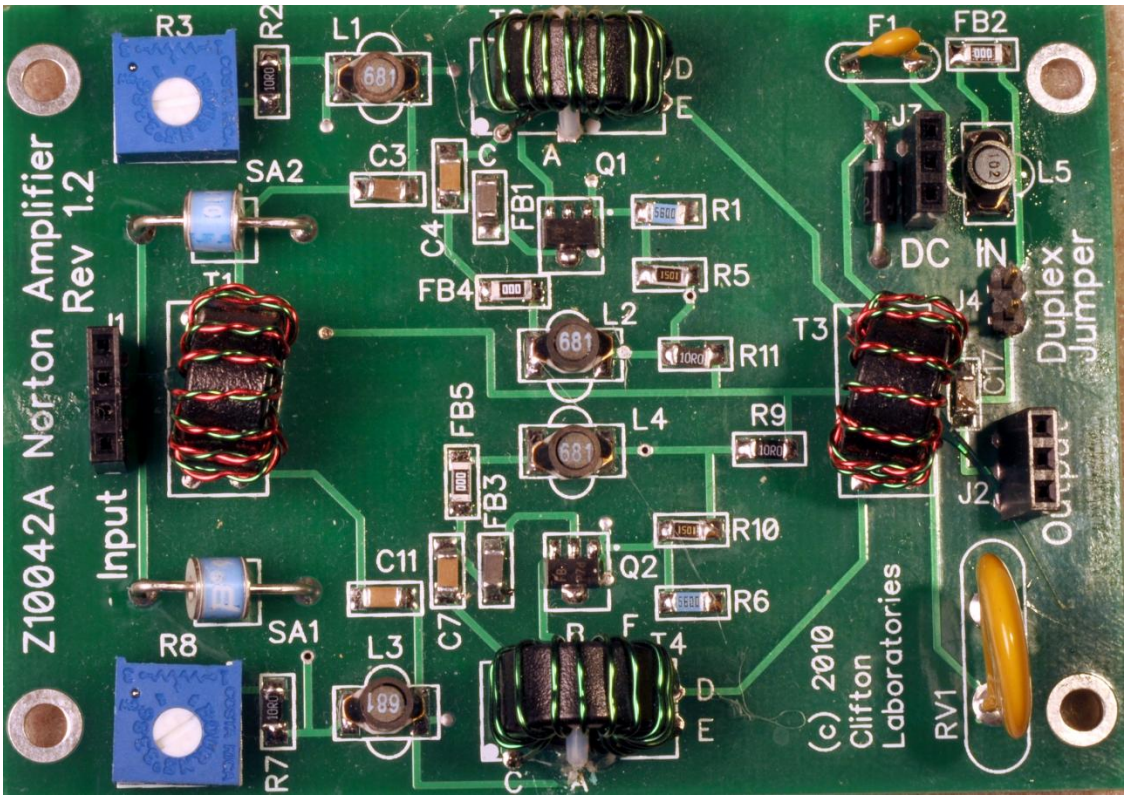
Route the wire through T2's center opening and to pads A and B as shown in the photographs below. You may find it easier to form the wire into a "U" form before installing it. When properly installed, the Teflon wire will hold the transformer core in place mechanically against the foam tape and PCB.



❑

Repeat this process for T4 with the second transformer.

At this point, all components should be installed and your Z10042A should resemble the one shown below.


Z10042A Norton Amplifier
Rev 1.2
Input
Duplex Jumper
Output
DC IN
(c) 2010
Clifton
Laboratories
R3
R2
L1
F1
FB2
SA2
C3
C4
FB1
Q1
R1
R5
FB4
L2
R11
T3
J4
C17
FB5
L4
R9
FB3
R10
C11
Q2
R6
SA1
R8
L3
C7
T4
R7
RV1
J2
L5
J1
T1

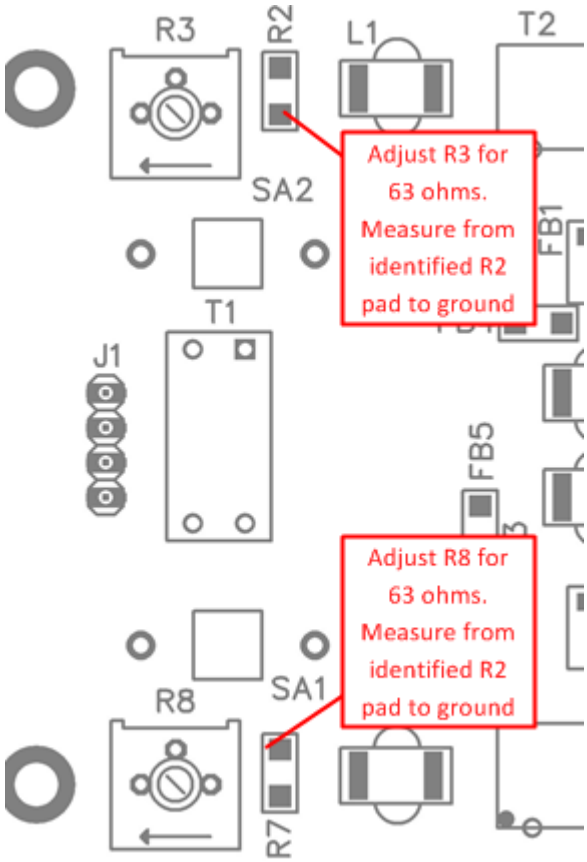
Post Construction Adjustment and Checkout

Before powering up the Z10042A, take a moment to make resistance checks and pre-set R3 and R8.

❑ With an ohmmeter measure and adjust R3 and R8 to 63± 2 ohms. (Both measuring points are with respect to ground, with the negative lead of the ohmmeter to ground.)

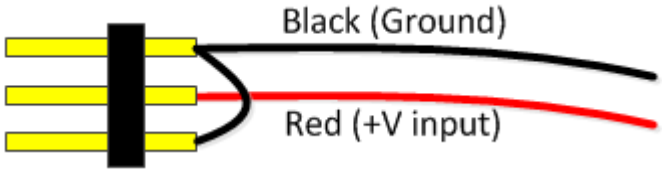
R3: Measuring point is junction of R3 and R2, as illustrated to the right.

R8: Measuring point is junction of R8 and R7 as illustrated to the right.



You may wish to make a complete set of resistance measurements as developed in the maintenance section of this manual.

❑ If you have not already done so, make up a power cable using a three-pin male header pin. Positive to the center pin and negative to the two outside pins.



❑ The Z10042A will work with DC supply voltages up to 15V and down to 12V. Performance data is based upon 13.8V DC.

⚠ The high performance transistors in the Z10042A are not as resistant to over-voltage as the through-hole parts used in the Z10040B Norton Amplifier. Accordingly, do not exceed 13.8V supply.

⚠ If a laboratory power supply with current limiting is available, set it for a maximum short circuit current of 175 mA and set the voltage to 0V. Connect the supply to the Z10042A at J3 (J4 duplex jumper open) and bring up the voltage slowly whilst observing the current. With R3 and R8 set for 63 ohms, the maximum current observed should be approximately 100 mA at 13.8V. If significant deviations from this value are observed, immediately remove power and investigate.

Adjusting R3 and R8. With the normal DC supply voltage applied through J3 (J4 duplex jumper open) preferably with a laboratory power supply with current limiting set to 175 mA, adjust R3 and R8.

⚠ Note: If you adjust R3 or R8 to the zero ohms extreme, it may be possible to damage components in the Z10042A. Some current limiting is built into the circuit, via R2 and R7, together with the resistance of L1 and L3. However, in order to provide the maximum adjustment range to compensate for variations in Q1 and Q2, complete protection against mis-adjustment is not possible. Accordingly, when adjusting R3 and/or R8, it is imperative that you observe the total current being drawn by the amplifier, and, if possible, use a power supply with current limiting set to 175 mA.

In addition, heatsinking of Q1 and Q2 is limited to that provided by the printed circuit board.

Under no circumstances should Q1 or Q2 be biased to draw more than 60 mA each.

⚠ Clifton Laboratories recommends setting the idle emitter current to a nominal value of 37.5 mA (35 to 40 mA range) per transistor. Of course, if the idle current balance is adjusted for optimum OIP2 performance the two amplifier sections will likely have slightly different idle current values.

To measure the current through Q1 and Q2, measure the voltage drop across R2 and R7, 10

ohm resistors. The emitter current (in mA) through the transistor is 1000 x V/10.0 where V is the drop across R2 or R7 in volts, 1000 is to convert the result to mA and 10.0 is the resistance of R2 and R7.

For the recommended 37.5 mA idle current, the voltage drop across R2 and R7 should be 0.375 volts nominal and in the range between 0.350V and 0.400V.

- ❑ Alternative 1: If you do not have the ability to measure 3rd order and 2nd order intermodulation products, adjust R3 and R8 such that Q1 and Q2 have substantially equal emitter currents of approximately 37.5 mA each, using the method above.

- ❑ Alternative 2: Adjust R3 and R8 for best 3rd and 2nd order intermodulation performance using the test equipment configuration you normally use for these measurements. During the adjustment process do not exceed 60 mA in either Q1 or Q2 as it is possible to damage components with over-current.

  Clifton Laboratories does not recommend and is not responsible for damage to the Z10042A if the emitter current is set to exceed 60 mA per transistor. 37.5 mA should be the target.

  A bias adjustment service for kit builders not equipped to measure IP2 and IP3 is available. Contact Clifton Laboratories for details.

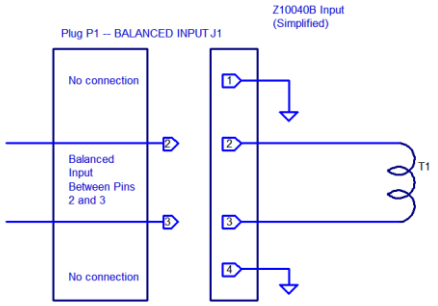
Input and Output Connections

Output and DC power connections are made to the Z10042A with 3-pin headers. Since the outside pins are always ground, either orientation is permitted. Input to the Z10042A is made with a 4-pin header and may be configured for either balanced or unbalanced input.

Balanced Input

To make a balanced connection to the Z10042A, use J1's two center pins, as illustrated in the drawing to the right.

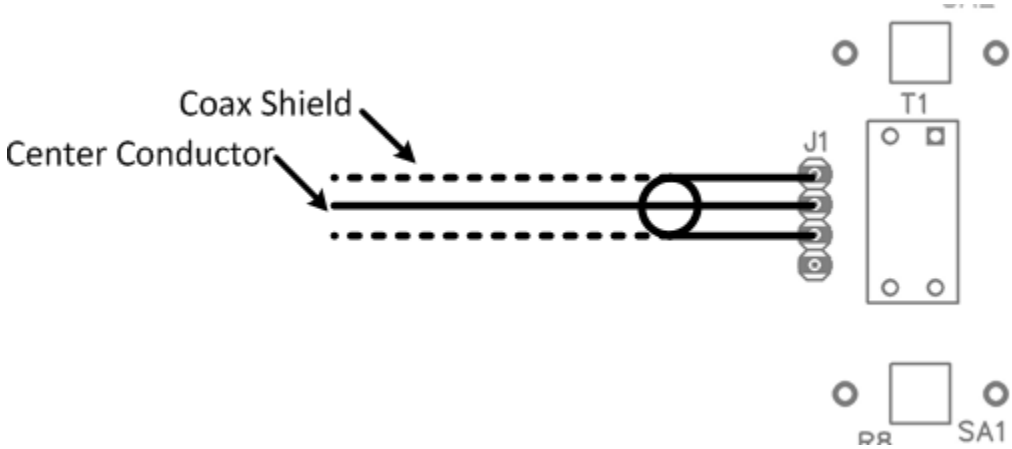
If a shielded pair is used for the balanced input, the shield should be connected to the two outside pins, which are common with the Z10042A's ground plane.



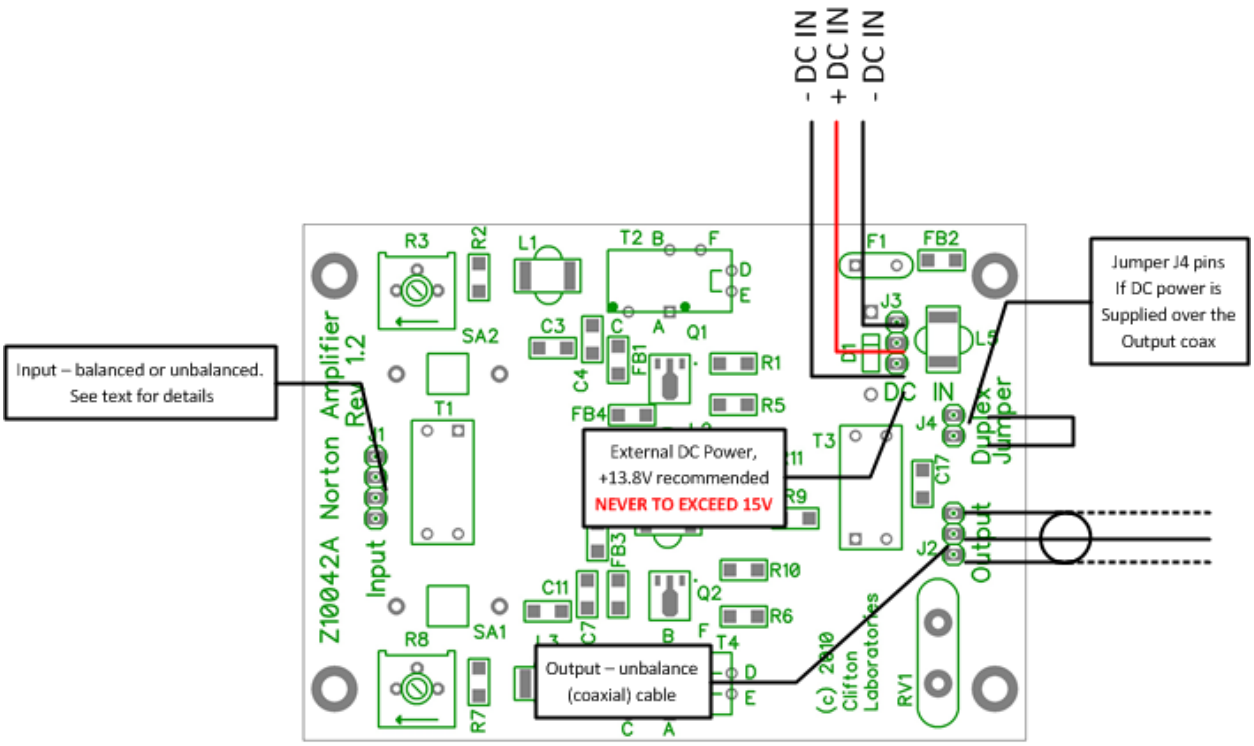
Unbalanced Input

Unbalanced (coaxial cable) input can be made to the Z10042A as illustrated below.

As always when making connections to a high gain amplifier, shielded coaxial cable should be used on the output (and the input if unbalanced) and the output cable should not be routed near the input. If balanced input is used, the input cable should be twisted pair or shielded pair to avoid unwanted signal pickup or feedback and oscillation.



Connections Diagram



This completes the assembly and verification of your Z10042A Norton Amplifier.

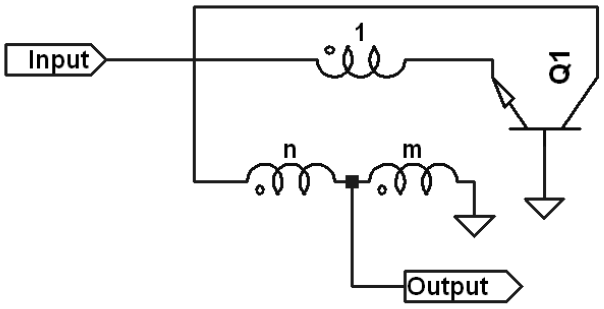
Schematic and Theory of Operation and Troubleshooting

Theory of Operation

The Z10042A Norton amplifier consists of two identical amplifier sections arranged in push-pull.

The discussion below uses component designations for the section associated with Q1.

Each section is a common base (also known as "grounded base") amplifier. As such, essentially identical signal currents flow through all three sections of T2 and T1's secondary winding. Gain is achieved in the grounded base amplifier because the collector load, represented by T2's n and m windings operating as an auto-transformer has greater impedance than the emitter input, and hence power gain results.



The figure at the right is a simplified view of an amplifier section, with all DC biasing and blocking components removed so that we may concentrate on the signal flow. The transformer turns ratios are shown as 1:n:m, but this does not mean the emitter feedback winding must have only one turn. Rather, it is the ratio of turns that is important, so that if the emitter winding has, for example, two turns, then the number of turns in windings n and m should also be doubled.

Consider windings n and m and assume a load of impedance Z is connected from output to ground. Windings n and m form an auto-transformer with Q1's collector seeing an impedance of:

$$Z_C = Z_O\left(\frac{n+m}{m}\right)^2$$

Since the same signal current flows through the emitter and collector (neglecting base current), the gain of the common base amplifier is proportional Zc or n and m in this relationship.

The transformer turns ratios should not be arbitrarily selected, if the full benefits of the Norton amplifier are to be realized. From Patent No. 3,891,934, the following equation governs the transformer turns relationship:

$$n = m^2\left(\frac{R_S}{R_L}\right) - m - 1$$

$$n = m^2 \left(\frac{R_S}{R_L}\right) - m - 1$$

Where

R_S is the source (input) impedance

R_L is the load (output) impedance

n and m are the transformer winding ratios, normalized to an emitter winding with one turn.

In our case, we wish the input and output impedances to be equal, and hence $R_S/R_L = 1$. Thus the turns relationship is simplified to:

$n = m^2\text{-}m\text{-}1$

The amplifier's transducer gain[1] is stated as:

$$G_t = m^2 \frac{R_S}{R_L}$$

Again, since our normal operation is with equal input and output impedances, the transducer gain G_t is simply m^2.

Winding Ratio 1:n:m	Transducer Gain (dB)
1:1:2	6.0
1:5:3	9.5
1:11:4	12.0
1:19:5	14.0
1:29:6	15.6

These figures are theoretical and the actual realizable gain is typically a dB or so less. See Appendix F for measured data on a 1:29:6 amplifier.

One significant advantage of the Norton amplifier is that the input impedance automatically tracks the output impedance. Thus, if terminated into a 50 ohm load, the input impedance is 50 ohms. If the output impedance is changed to 75 ohms, the input impedance becomes 75 ohms. (This relationship is again not perfect, but it is reasonably good with less than a 2:1 VSWR over the range 300 KHz – 30 MHz when measured in a 50 ohm system.)

DC power may be provided to the Z10042A via two feed points. First, a three-pin connector permits direct DC power connection. Secondly, adding a jumper at connector J4 permits DC power to be duplex fed over the coaxial cable transmission line carrying the amplifier's output. Of course, an

1 Transducer gain is defined as: "the ratio of the power delivered by a network to a load (PdL) to the power available from the source (Pas). Transducer gain is a function of the source and load reflection coefficients and the network s-parameters." http://www.maurymw.com/support/faqs/faqs/faq9.html

appropriate DC power injector, such as Clifton Laboratories model Z1203A, will be required and the power source that is used should be selected to have low noise at the frequencies of interest.

Over current protection is provided by F1, a 200 mA positive temperature coefficient "polyfuse." Should the amplifier draw more than 200 mA, F1 will heat and switch to a high resistance state, thereby limiting the current drawn by the power source. So long as the voltage remains applied, F1 will remain in the high resistance state.

Over voltage protection is provided by RV1, an 18V DC (nominal) bipolar metal oxide varistor. The primary purpose of RV1 is to limit damage to the DC power source, should a nearby lightning strike or other incident induce a greater than normal voltage on the DC power line. Although RV1 is rated to begin clamping at 18V (1.0 mA clamp current at 18V), the actual onset voltage may be 20% above this figure and the clamping voltage may rise as high as 36V at 50A clamping current. Hence, even with RV1 in place and functioning properly, excessive over voltage may still occur if the disturbing event is sufficiently energetic. (The ROV14-180M device used in the Z10042A is rated at a one-time 1,000A clamp or two-times 500A clamp. However, at 1000A, the expected clamping voltage is 80V.)

Reverse voltage protection is provided by D1, a 1N400x series diode connected to be forward biased if the input polarity reverses. This causes two things to happen. First, the maximum voltage across the DC power distribution circuitry will be limited to approximately 1V by D1. Secondly, fuse F1 will enter into high resistance mode by virtue of the over current. Of course, a sufficiently robust power supply connected with reverse polarity may destroy D1 before F1 can enter high resistance mode.

The Z10042A's input is through a bifilar wound, broadband transformer, T1. Both of T1's primary terminals are brought out to J1 through K1's contacts so that either balanced or unbalanced input may be used. Balanced input signals are applied across T1's primary, which remains floating with respect to ground. If unbalanced input is used, one of T1's primary terminals is connected to ground through appropriate jumper settings at J1, or via the ground connection modification discussed in the assembly section of this manual.

Ferrite beads FB1 and FB3, along with C22 and C23 prevent VHF/UHF parasitic oscillations. (The NE85634 transistors have appreciable gain above 5 GHz.)

DC power is supplied to Q1 and Q2 through RF chokes L2 and L4, with T2 and T4 output sections being AC coupled by blocking capacitors C4 and C7. There is thus no DC current flowing in T2 and T4's windings, except for the emitter current through the one turn input winding. Removing DC current from T2 and T4 from the majority of the windings reduces core saturation and improves low frequency performance.

The Z10042A's input circuit is protected in two ways. First, when DC power is removed from the Z10042A, relay K1 removes the input connection and connects it to ground through R4 and R12, 49R9 ohm resistors. (If desired, the user may replace R4 and R12 with wire jumpers to the input when power is removed.) Secondly, SA1 and SA2, "gas trap" or spark protector devices are always connected across the Z10042A's input connector. Although SA1 and SA2 limit the voltage for fast

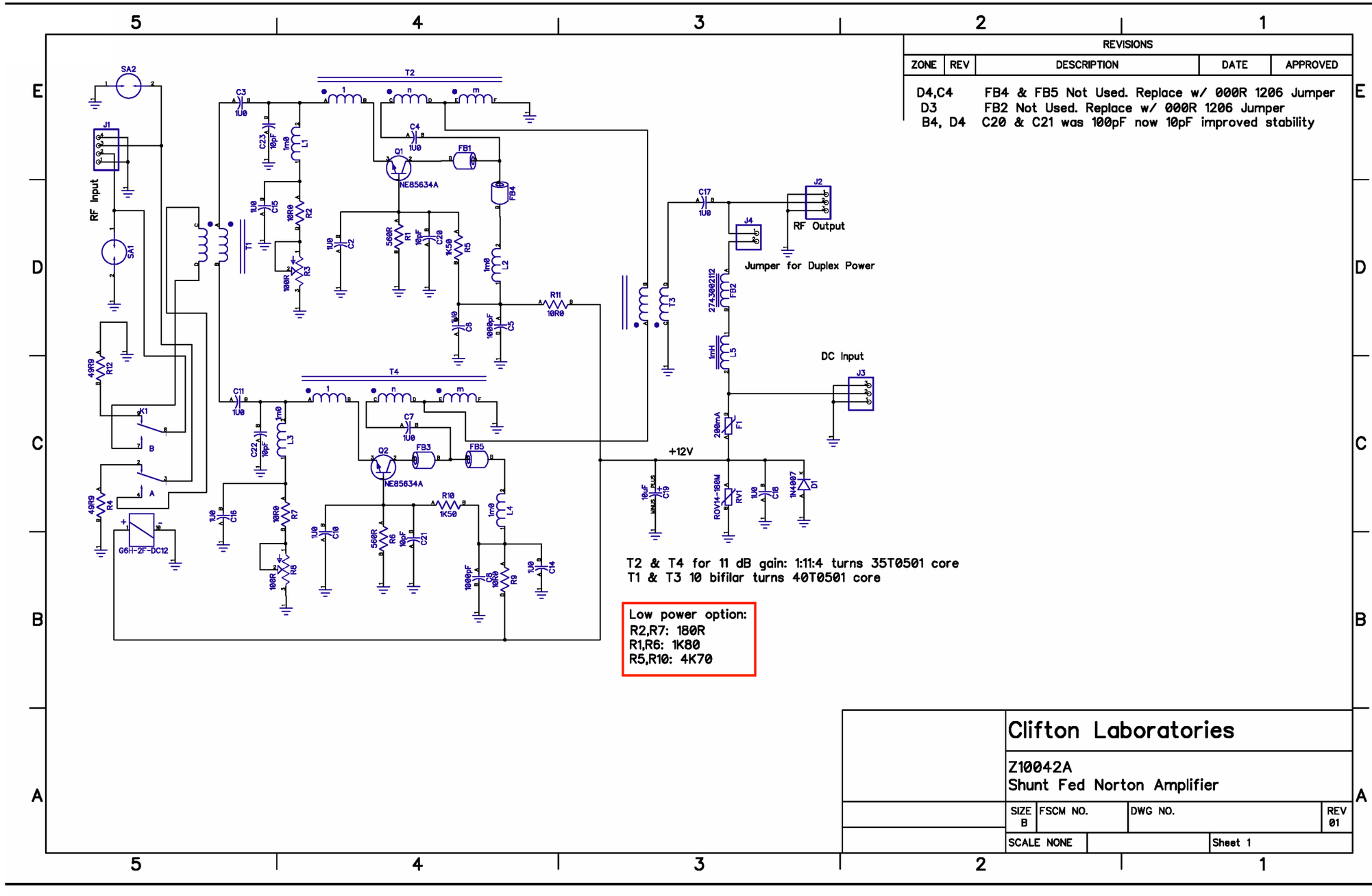
rise time pulses, their break over voltage may be several hundred volts. The primary purpose of SA1 and SA2 is to limit the voltage that might otherwise be coupled over the coaxial transmission line and, secondarily, to provide some protection to the Z10040's components.

When the input is configured as unbalanced, only one of SA1 and SA2 is operational. In balanced mode, SA1 and SA2 are connected between the two balanced inputs and the Z10042A's common ground point. Likewise in balanced mode, when the Z10042A is unpowered, R4 and R12 are connected across the balanced input to the Z10042A's common ground point.



All of these protection measures assume that the Z10042A is properly grounded and that good engineering practices have been used in its installation and construction of the ground system. The Z10042A is not intended to survive a direct lightning strike to an antenna connected to its input, whether powered up or not. However, the protective measures incorporated into the Z10042A's design should aid in reducing damage, particularly where the strike is not directly to the antenna system.

Schematic



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
D4,C4		FB4 & FB5 Not Used. Replace w/ 000R 1206 Jumper		
D3		FB2 Not Used. Replace w/ 000R 1206 Jumper		
B4, D4		C20 & C21 was 100pF now 10pF improved stability		

Clifton Laboratories				
Z10042A Shunt Fed Norton Amplifier				
SIZE B	FSCM NO.	DWG NO.		REV 01
SCALE NONE			Sheet 1	

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
D4,C4		FB4 & FB5 Not Used. Replace w/ 000R 1206 Jumper		
D3		FB2 Not Used. Replace w/ 000R 1206 Jumper		
B4, D4		C20 & C21 was 100pF now 10pF improved stability		

Z10042A Typical Voltage and Current Values
Test Conditions:
1. 13.80 V supply
2. R3 and R8 adjusted for approximately 38 mA emitter current Q1 & Q2

15mA — Current in mA

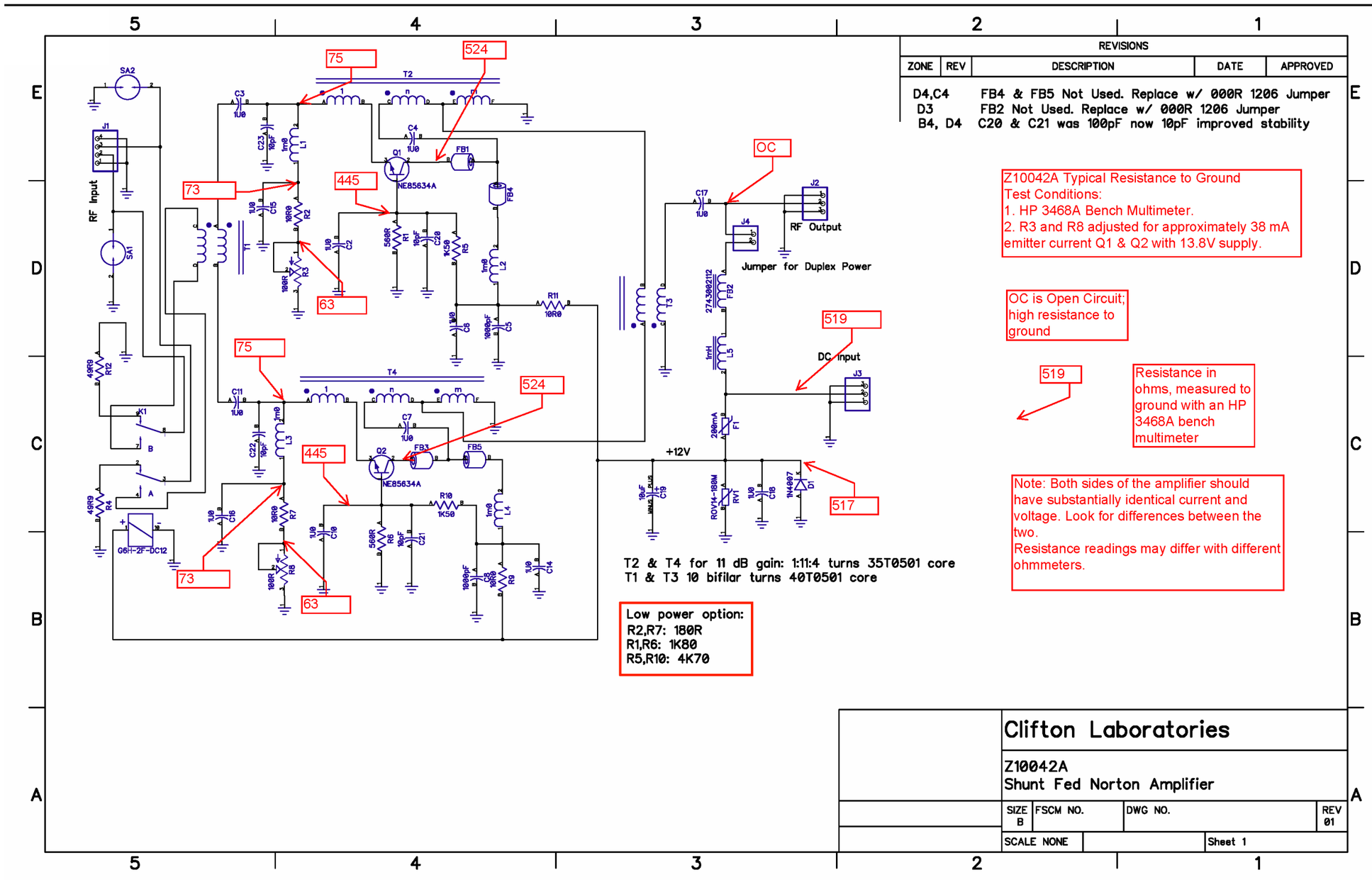
13.80 — Voltage in volts

Note: Both sides of the amplifier should have substantially identical current and voltage. Look for differences between the two.

T2 & T4 for 11 dB gain: 1:11:4 turns 35T0501 core
T1 & T3 10 bifilar turns 40T0501 core

Low power option:
R2,R7: 180R
R1,R6: 1K80
R5,R10: 4K70

	Clifton Laboratories			
	Z10042A Shunt Fed Norton Amplifier			
	SIZE B	FSCM NO.	DWG NO.	REV 01
	SCALE NONE		Sheet 1	


5
4
3
2
1
E
D
C
B
A
SA2
J1
RF Input
SA1
K1
G6H-2F-DC12
T2
T4
T1
T3
Q1
Q2
NE85634A
FB1
FB3
FB4
FB5
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
L1
L2
L3
L4
L5
J2
RF Output
J4
Jumper for Duplex Power
J3
DC Input
FT
RV1
D1
1N4007
+12V
OC
519
517
524
445
75
73
63
T2 & T4 for 11 dB gain: 1:11:4 turns 35T0501 core
T1 & T3 10 bifilar turns 40T0501 core
Low power option:
R2,R7: 180R
R1,R6: 1K80
R5,R10: 4K70
REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPROVED
D4,C4 FB4 & FB5 Not Used. Replace w/ 000R 1206 Jumper
D3 FB2 Not Used. Replace w/ 000R 1206 Jumper
B4, D4 C20 & C21 was 100pF now 10pF improved stability
Z10042A Typical Resistance to Ground
Test Conditions:
1. HP 3468A Bench Multimeter.
2. R3 and R8 adjusted for approximately 38 mA emitter current Q1 & Q2 with 13.8V supply.
OC is Open Circuit; high resistance to ground
519
Resistance in ohms, measured to ground with an HP 3468A bench multimeter
Note: Both sides of the amplifier should have substantially identical current and voltage. Look for differences between the two.
Resistance readings may differ with different ohmmeters.
Clifton Laboratories
Z10042A
Shunt Fed Norton Amplifier
SIZE B | FSCM NO. | DWG NO. | REV 01
SCALE NONE | Sheet 1

Appendix A Typical Performance Data

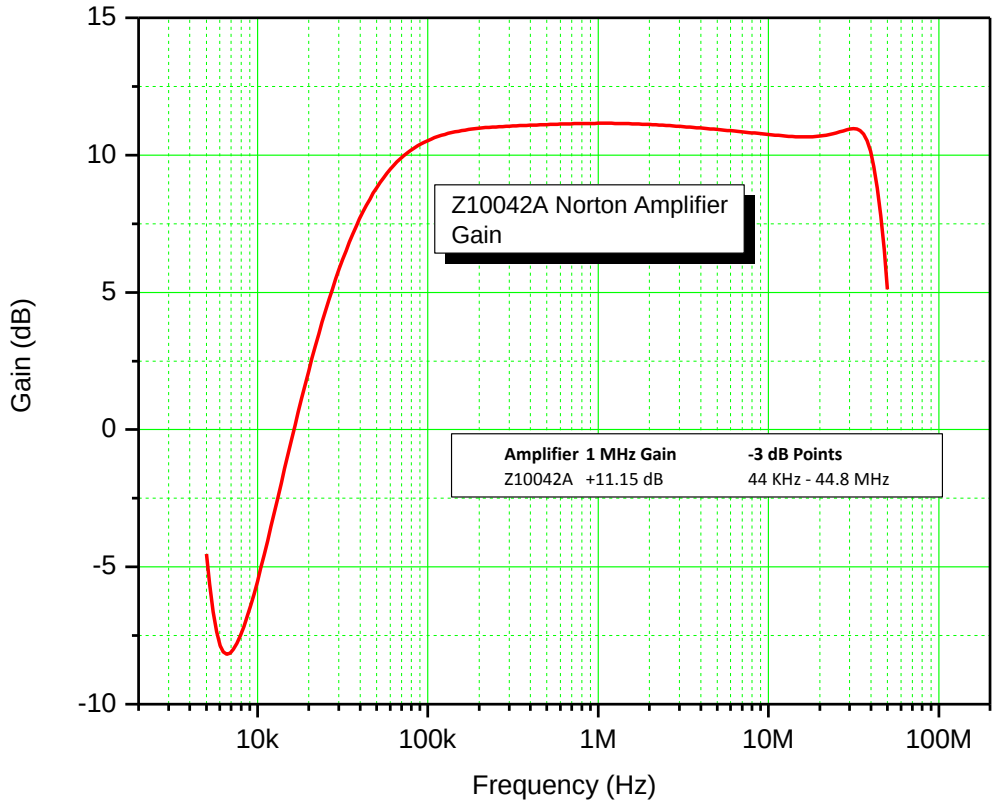
Except for common mode rejection, the data presented below is taken from one Z10042A amplifier.

While it is believed representative of Z10042A amplifiers, due to component tolerance, assembly practices and test setup, the performance level seen in these measurements should be regarded as *typical* and is not guaranteed.

Unless otherwise specifically noted, the data is taken with unbalanced input.

Bandwidth

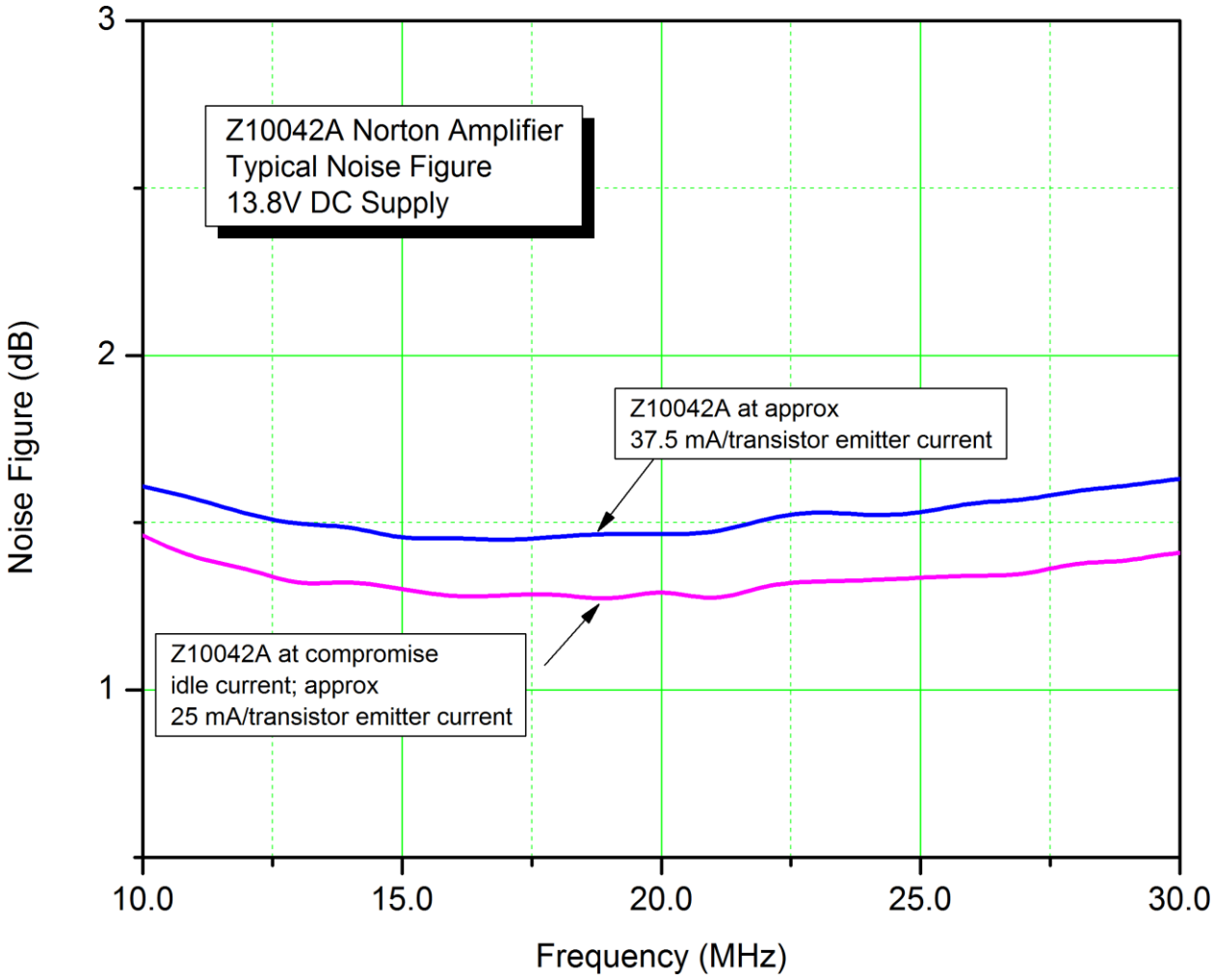
Test Conditions: Direct DC feed.



Noise Figure

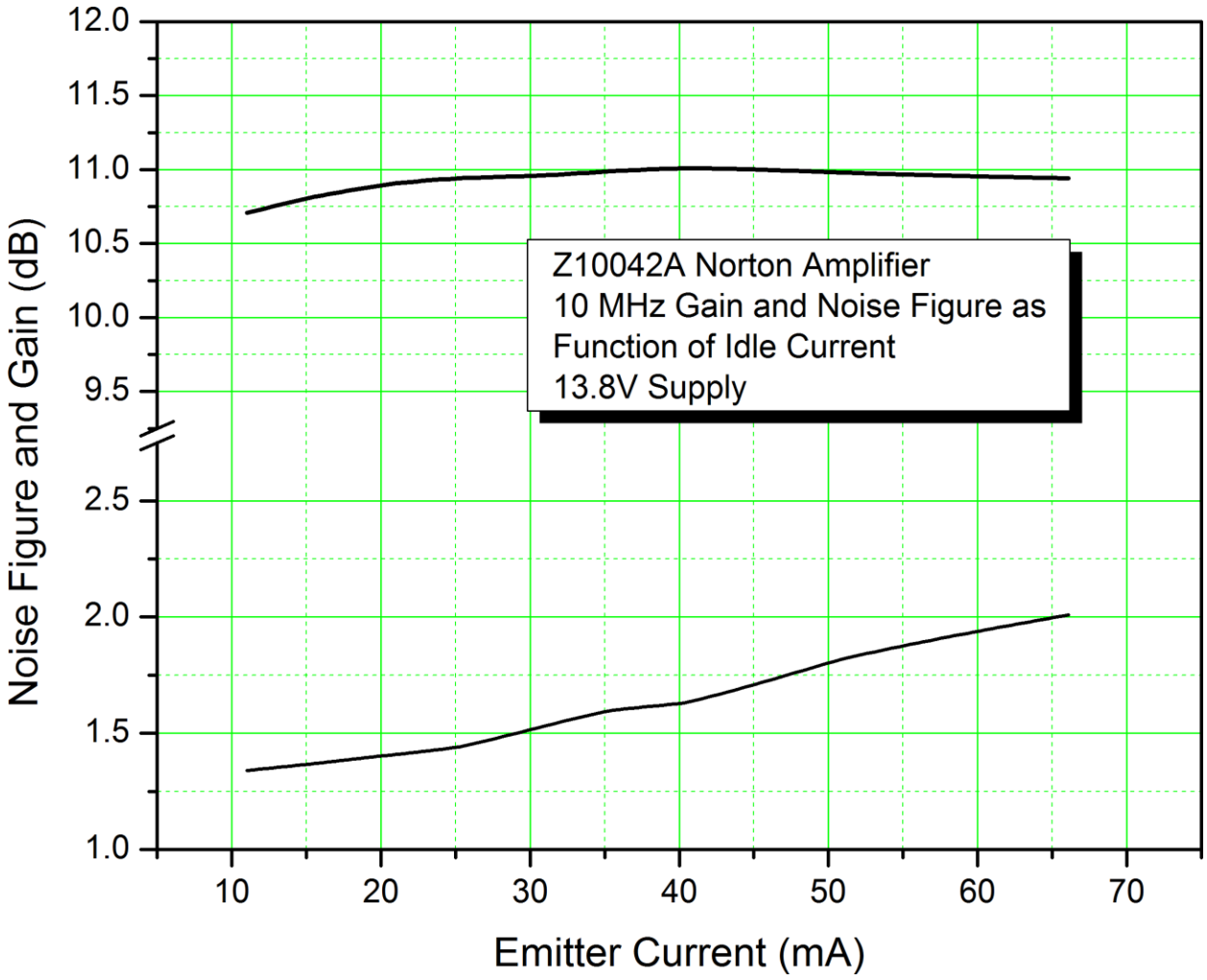
NF versus Frequency

Data taken with an HP8970A noise figure meter and AIL 7615 noise source at 13.8V supply.



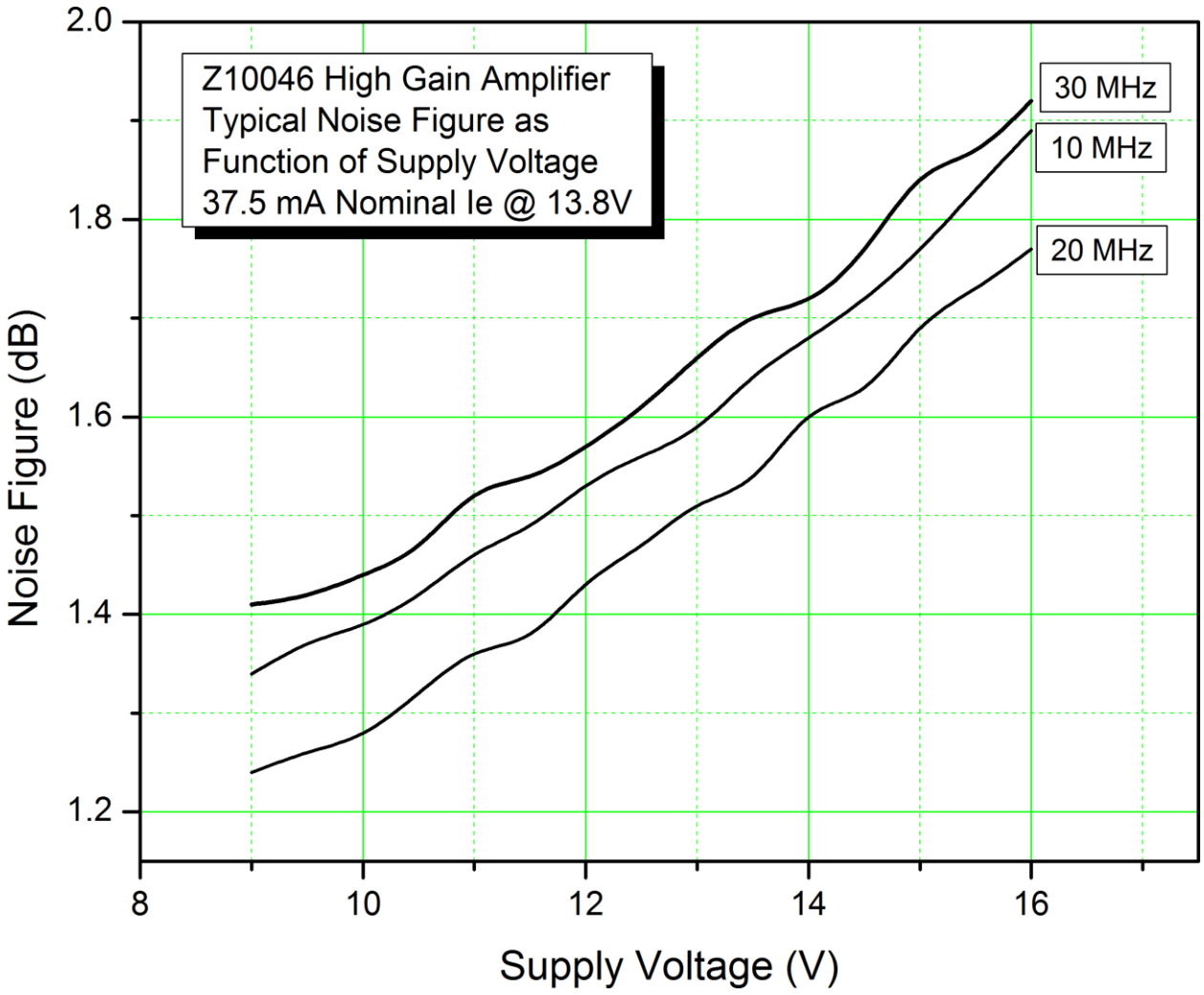
NF and Gain versus Idle Current

Test conditions: 13.8V supply voltage. Idle current adjusted between 11 mA and 66 mA. Noise figure and gain measured at 10 MHz with an HP8970A noise figure meter and AIL 7615 noise source.



NF as function of supply voltage

Test conditions: Idle current adjusted for approximately 37.5 mA emitter current (each transistor); supply voltage varied between 9 and 16V. Noise figure measured at 10, 20 and 30 MHz with an HP8970A noise figure meter and AIL 7615 noise source.

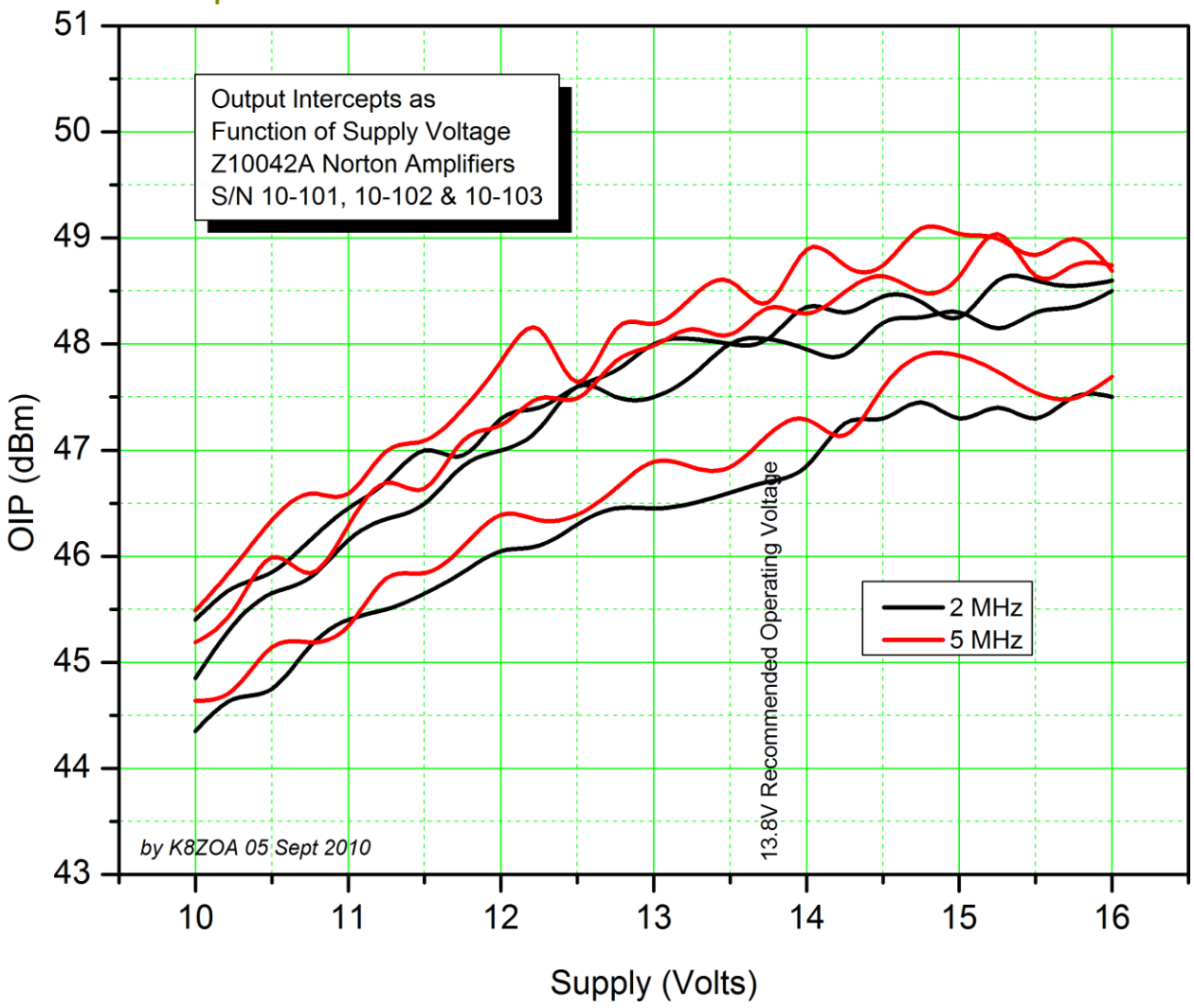


Second and Third Order Intermodulation

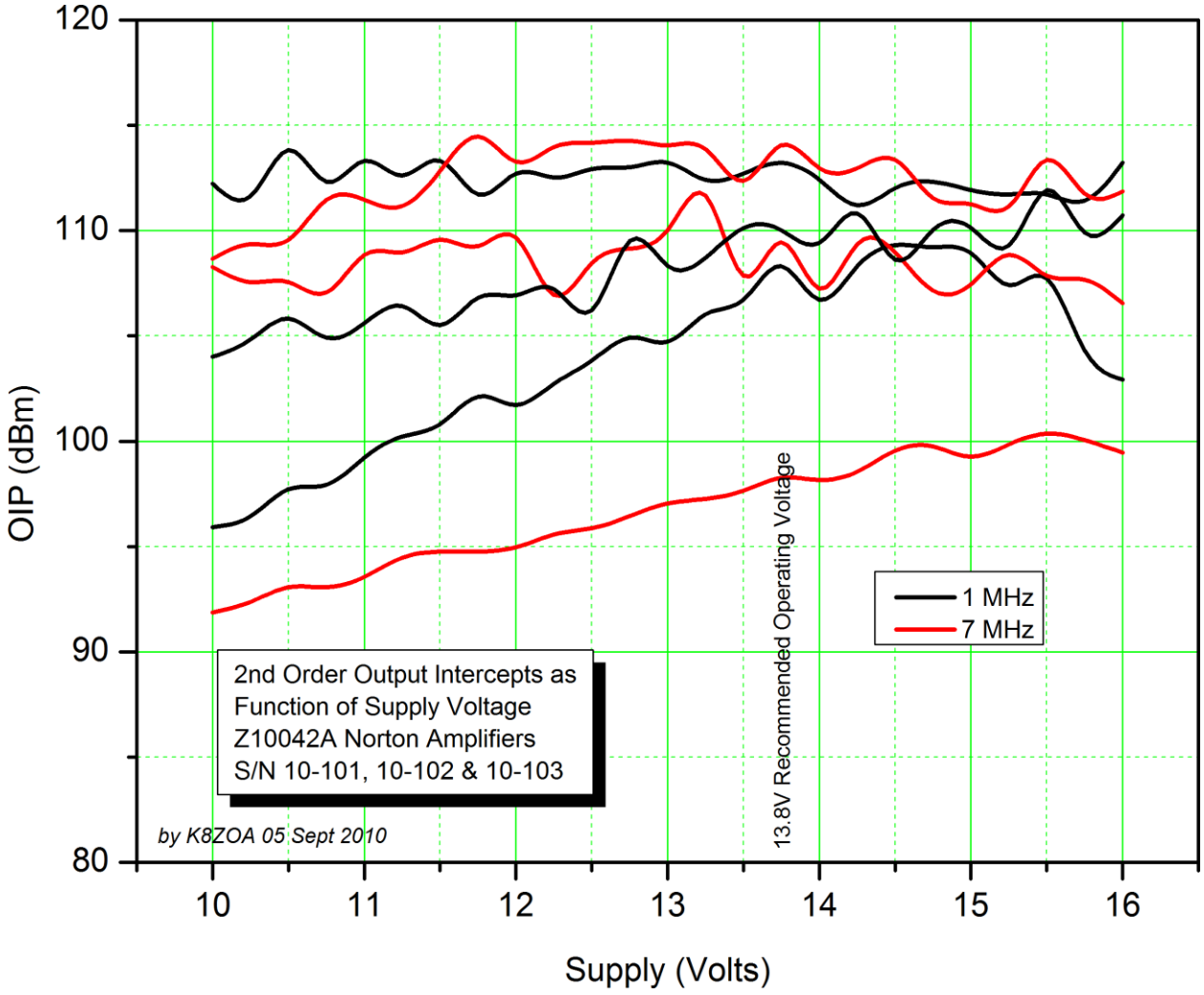
Test conditions: Three Z10042A amplifiers of consecutive serial number tested. Each adjusted for optimum OIP2 with 13.8V DC supply voltage and emitter current 37.5 mA per transistor (approximately). Supply voltage adjusted between 10.0V and 16.0V and 2nd and 3rd order intercepts measured. Two test signals at 3007 KHz and 4011 KHz, adjusted to provide an output level of 0 dBm for each tone.

OPERATIONS AT VOLTAGES ABOVE 15.0V ARE NOT RECOMMENDED AND ARE EXCLUDED FROM WARRANTY.

3rd Order Intercept

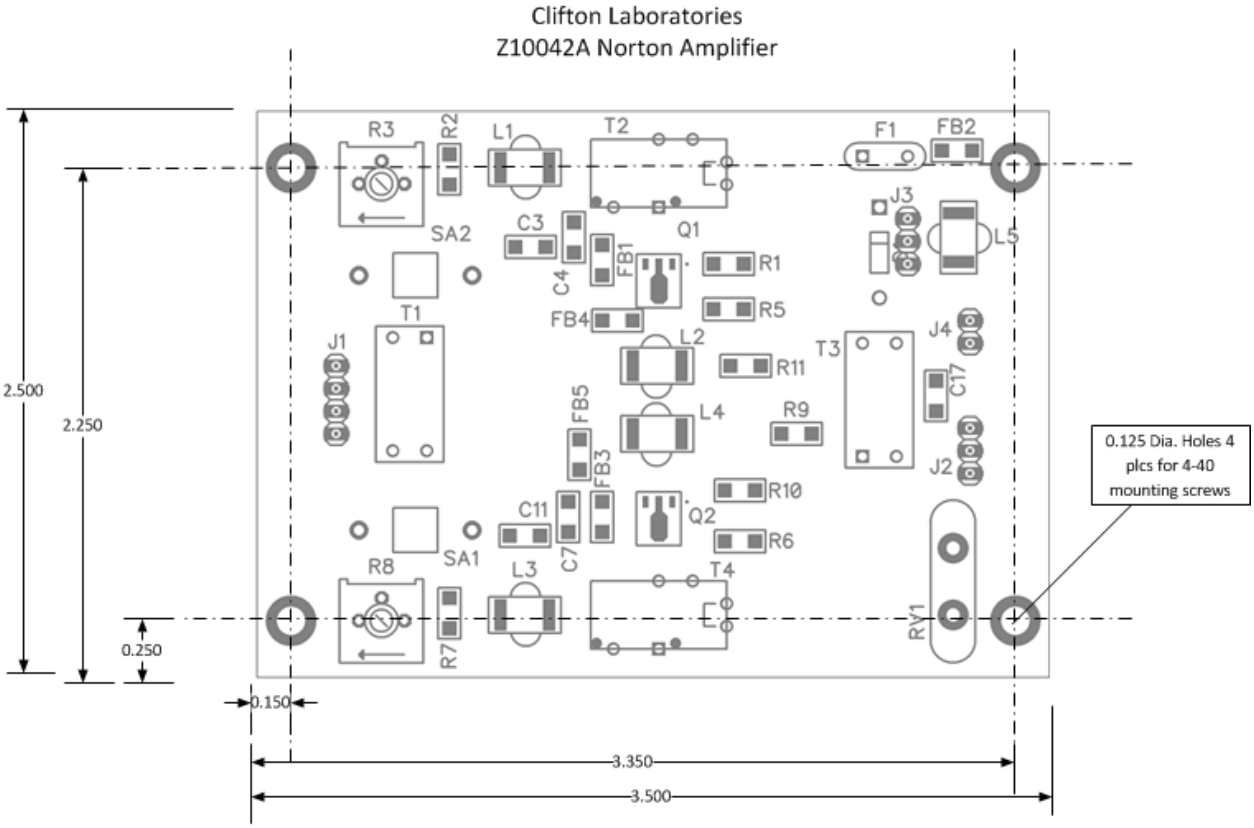


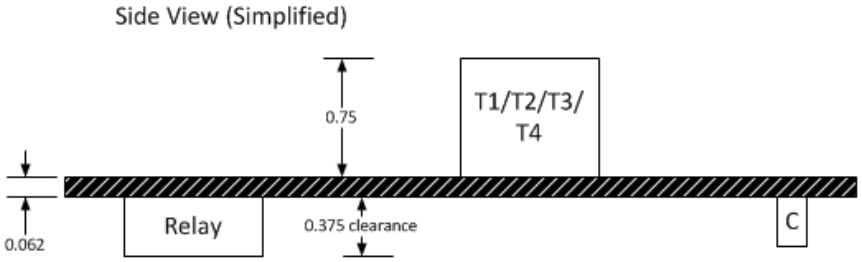
2nd Order Intercept



Appendix B – PCB Mounting Hole Dimensions

Drawing is **not** to scale. There is no change in mounting hole spacing and size between the Z10040A and Z10042A.





25 May 2010
NOT TO SCALE
All dimensions in inches

Appendix C – Norton Amplifier Patent, US Patent No. 3,891,934

United States Patent [19]

Norton et al.

[11] **3,891,934**

[45] **June 24, 1975**

[54] **TRANSISTOR AMPLIFIER WITH IMPEDANCE MATCHING TRANSFORMER**

[75] Inventors: **David E. Norton**, Framingham, Mass.; **Allen F. Podell**, Los Altos, Calif.

[73] Assignee: **Adams-Russell Co., Inc.**, Waltham, Mass.

[22] Filed: **May 22, 1974**

[21] Appl. No.: **472,281**

[52] **U.S. Cl.** **330/21**; 330/19; 330/26; 330/165; 330/188; 330/195

[51] **Int. Cl.** **H03f 3/04**

[58] **Field of Search** 330/12, 19, 21, 22, 40, 330/165, 188, 195

[56] **References Cited**

UNITED STATES PATENTS

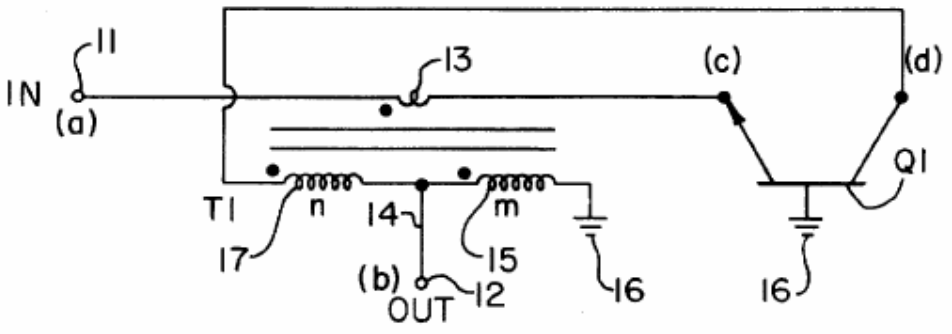
2,691,077	10/1954	Koros	330/40 X
2,701,281	2/1955	DeWhite et al.	330/12 X

Primary Examiner—R. V. Rolinec
Assistant Examiner—Lawrence J. Dahl
Attorney, Agent, or Firm—Charles Hieken, Esq.; Jerry Cohen, Esq.

[57] **ABSTRACT**

An amplifier includes a transistor and transformer having a primary winding and a tapped secondary winding. The primary winding is connected in series between the input terminal and the transistor emitter. The transistor base and one end of the secondary winding is grounded. The other end of the secondary winding is connected to the transistor collector. The transformer secondary tap is connected to an output terminal. The ratio of that portion of the secondary turns connected between the tap and *r-f* ground and the primary turns is m. The ratio of that portion of the secondary turns connected between the tap and the transistor collector and the primary turns is n. For two-way impedance match between a source resistance R_s and a load resistance R_L, $n = m^2 (R_s/R_L) - m - 1$.

8 Claims, 5 Drawing Figures



1

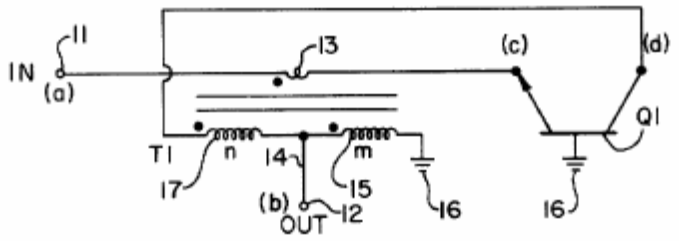


FIG. 1

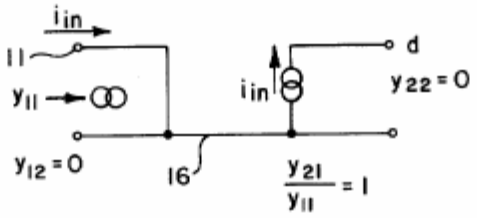


FIG. 2

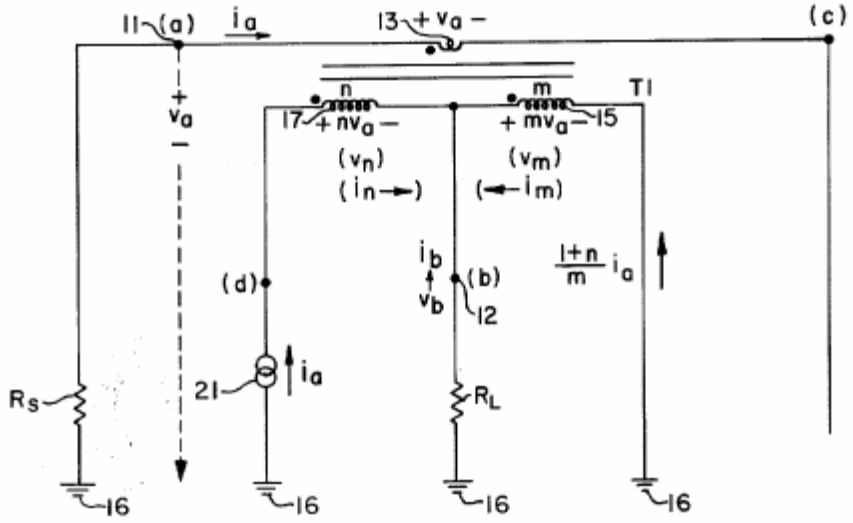


FIG. 3

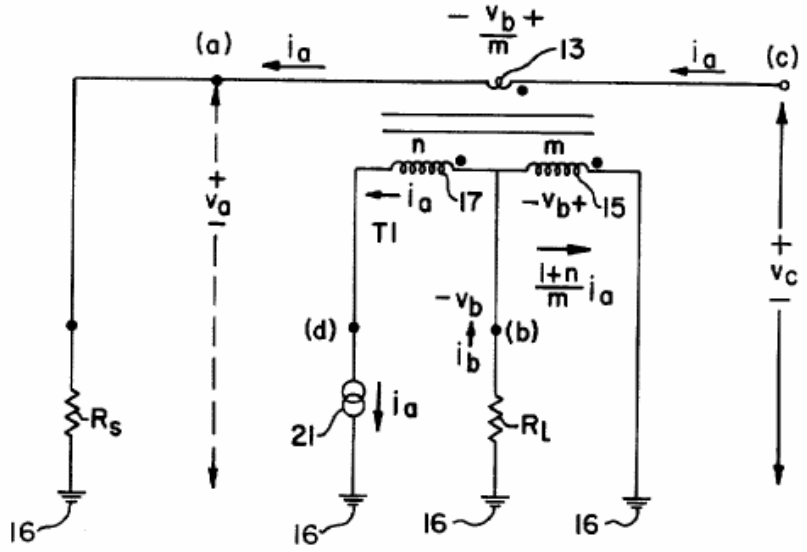

(a)
i_a
$-\frac{v_b}{m}+$
13
i_a
(c)
n
m
$+v_a-$
i_a
17
$-v_b+$
15
T1
$\frac{1+n}{m} i_a$
$+v_c-$
$-v_b$
(d)
(b)
i_b
i_a
R_S
21
R_L
16
16
16
16

FIG. 4

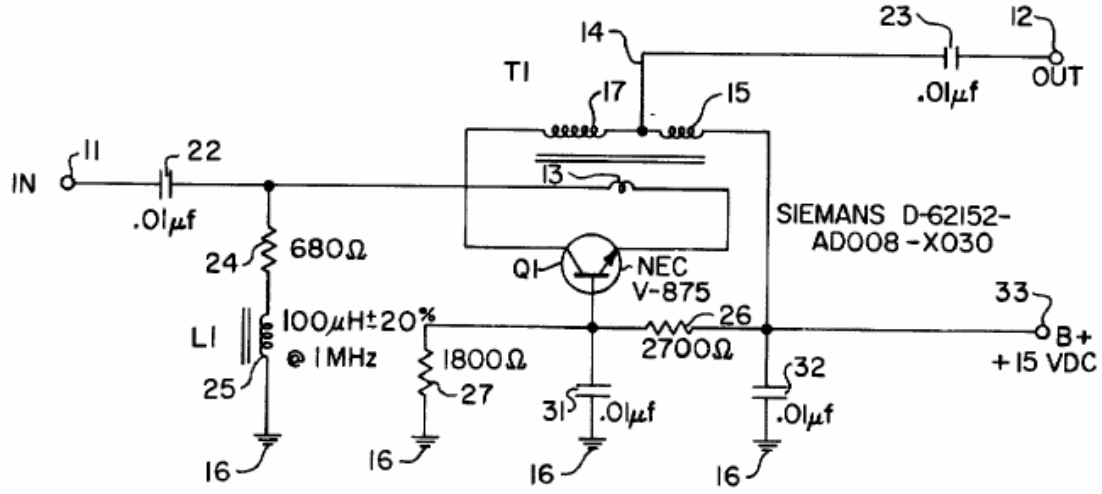

14
23
12
T1
17
15
.01μf
OUT
IN
11
22
13
.01μf
SIEMANS D-62152-
AD008-X030
24
680Ω
Q1
NEC
V-875
33
L1
100μH±20%
@ 1MHz
26
2700Ω
B+
+15 VDC
1800Ω
27
32
25
31
.01μf
.01μf
16
16
16
16

FIG. 5

TRANSISTOR AMPLIFIER WITH IMPEDANCE MATCHING TRANSFORMER

BACKGROUND OF THE INVENTION

The present invention relates in general to ampifying and more particularly concerns a novel amplifier with high dynamic range and efficiency especially useful in matching both a source impedance and a load impedance while providing *r-f* amplification over a relatively broad band with a single transformer and single transistor.

CATV coaxial cable systems that transmit and amplify television signals use many amplifiers representing a significant cost of the system. To avoid reflections that cause undesirable visible ghosts on a television screen, care is taken to properly terminate the transmission lines. Thus, both the input and output of an amplifier should match that of the transmission line to which it is connected. While techniques for achieving this result are known, conventional prior art circuits involve many components that are relatively costly to acheive this result.

Still another problem arises from the range of signal levels to be amplified. It is difficult to amplify low level signals adequately and avoid overloading the amplifier with high level signals. Furthermore, dissipation of *r-f* power in amplifying circuit resistors reduces efficiency.

Accordingly, it is an important object of this invention to provide an economical low-noise *r-f* amplifier with high dynamic range and efficiency capable of conveniently matching both a source impedance and a load impedance while providing good amplification over a relatively broad bandwidth.

It is another object of the invention to achieve the preceding object with relatively few components.

It is a further object of the invention to achieve one or more of the preceding objects with relatively few components, none of which need be adjusted once circuit design is complete.

It is still a further object of the invention to achieve one or more of the preceding objects with a circuit that has only one transistor and one transformer.

SUMMARY OF THE INVENTION

According to the invention, there is an amplifying device having control, input and output electrodes, such as a transistor having at least base, emitter and collector electrodes. Means are provided for effectively connecting at *r-f* the control electrode or base to a common or reference terminal. Transformer means having at least a primary winding and a tapped secondary winding has the primary winding coupled in series between an input terminal and the imput electrode or emitter and its secondary winding effectively coupled between the common terminal and the transistor collector. An output terminal is coupled to a tap between first and second portions of the transformer secondary winding, the first portion being coupled between the tap and the common terminal. The ratio of first portion turns to primary turns is m; of second portion turns to primary turns, *n*. Preferably $n = m^2(R_s/R_L) - m - 1$ where R_s and R_L are the source and load resistances to be matched at the input and output terminals, respectively.

Numerous other features, objects and advantages of the invention will become apparent from the following

specification when read in connection with the accompanying drawing in which:

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a schematic circuit diagram of an embodiment of the invention;

FIG. **2** is a representation of the transistor as an ideal common base circuit with various admittance parameters;

FIG. **3** is an equivalent circuit of the circuit of FIG. **1** helpful in understanding the mode of operation;

FIG. **4** is the circuit of FIG. **3** redrawn to help determine the source impedance presented to the emitter; and

FIG. **5** is a schematic circuit diagram of a preferred embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

With reference now to the drawing and more particularly FIG. **1** thereof, there is shown a schematic circuit diagram of an embodiment of the invention for providing gain between input terminal **11** and output terminal **12** while matching a source impedance R_s connected to input terminal **11** and a load impedance R_L connected to output terminal **12.** The circuit comprises transistors Q1 and transformer T1. So as not to obscure the principles of the invention the specific means for applying operating and biasing potentials to the particular circuit elements are not shown, those skilled in the art knowing how to supply these potentials. For example, the collector may recieve d-c operating potential through the secondary winding of transformer T1 from a d-c supply bypassed to ground by a suitable capacitor in a manner well-known in the art.

For convenience in the explanation which follows below input terminal **11,** output terminal **12,** the emitter and the collector are designated nodes *a*, *b*, *c* and *d*, respectively. The primary winding **13** is connected between input terminal **11** and the emitter. The secondary winding of transformer T1 has a tap **14** connected to output terminal **12** and a first portion **15** between tap **14** and ground, reference or common terminal **16** and a second portion **17** between tap **14** and the transistor collector. The base of transistor Q1 is effectively connected to ground terminal **16.** The winding polarities are indicated by the dots.

Referring to FIG. **2,** transistor Q1 is represented as an ideal common base circuit having an input admittance y_{11} between base and emitter that is infinite, and output admittance y_{22} between collector and ground that is zero, a reverse transfer admittance y_{12} that is zero and a ratio of forward transfer admittance y_{21} to input admittance y_{11} that is unity.

Referring to FIG. **3,** there is shown an ideal equivalent circuit of the amplifier with a source resistance R_s connected between input terminal **11** and ground **16,** a load resistance R_L connected between output terminal **12** and ground **16,** and transistor Q1 represented as an ideal current source **21** connected between ground **16** and node d delivering the same current i_a into node *d* that enters node a and produces a potential v_a across primary winding **13.** Voltages across portions **17** and **15** and the currents flowing in the various leads are as indicated in FIG. **3.**

The following relationships hold:

$$v_n = nv_a \tag{1}$$

$$v_m = mv_a \tag{2}$$

$$i_a + ni_n = mi_m \tag{3}$$

Since a flows through both the single primary turn and the n turns, then

$$i_m = [(1+n/m\ ]\ i_a$$

With the transformer ideal, and the dependent current generator at node d, the following relationships hold:

$$v_b = mv_a \tag{4}$$

$$i_b = -(i_n + i_m)$$

$$i_b = -\ [(m + n + 1)/\mathrm{m}]\ i_a \tag{5}$$

Hence

$$v_b\, i_a = -\ (m + n + 1)\ i_n v_a \tag{6}$$

$$v_b/i_b = -\ [m^2/(m+n+1)]\ v_a/i_a \tag{7}$$

With a voltage source in series with source resistance R_s, i_b flows outward into R_L, and

$$v_b/i_b = -R_L \tag{8}$$

Hence from (7)

$$v_a/i_a = [(m\ +n\ +1)/m^2\ ]\ R_L = R_{in} \tag{9}$$

With a voltage source in series with R_L, i_a flows outward into R_s, and

$$v_a/i_a = -R_s \tag{10}$$

Hence from (7)

$$v_b/i_b = [m^2/(m+n+1)]R_s = R_{out} \tag{11}$$

The input impedance matches the source resistance R_s if m and n are related by

$$R_{in} = R_s = [(m+n+1)/m^2]R_L \tag{12}$$

If this expression for R_s is substituted in equation (11), $R_{out} = R_L$, the desirable situation of two-way impedance match. Rewriting equation (12) to relate m and n for two-way impedance match,

$$n = m^2(\mathrm{R_s/R_L}) - m - 1 \tag{13}$$

Note that if m is an integer and R_s and R_L are related so that $m^2(R_s/R_L)$ is also an integer, then n will also be an integer.

It is assumed that equation (13) is satisfied from here on. With a voltage source, v, in series with R_s, then the available power at the input is

$$P_{av_a} = v^2/4R_s \tag{14}$$

But with equation (13) satisfied, the input is matched and

$$v_a = v/2 \text{ and } P_{av_a} = v_a i_a \tag{15}$$

The power delivered to the load at node b is

$$P_b = -v_b i_b = (m+n+1)\ P_{av_a} \tag{16}$$

The transducer gain G is the ratio of:

$$P_b/P_{av_a} = G = m+n+1 = m^2(R_s/R_L) \tag{17}$$

Likewise with the generator at node b we have

$$P_{av_b} = v^2/4R_L,\ v_b = v/2 \text{ and } v_b i_b = P_{av_b}$$

Hence:

$$P_a = -v_a i_a = [1/(m+n+1)]P_{av_b} \tag{18}$$

and the reverse gain G_r is given by

$$P_a/P_{av_b} = G_r = 1/G \tag{19}$$

With the source at node a the load impedance, R_{Lc}, presented to the collector is

$$R_{Lc} = v_a/i_a = [(n+m)\ v_a]/i_a \tag{20}$$

but $v_a/i_a = R_s$. Hence:

$$R_{Lc} = (n+m)\ R_s \tag{21}$$

Referring to FIG. **4**, the equivalent circuit of FIG. **3** is redrawn to facilitate determining the source impedance presented to the emitter as seen looking in at the emitter feed point between node c and ground **16**. Assuming that node c is positive with respect to ground, the voltages and currents are as indicated in FIG. **4** and the following relationships occur.

$$R_{sc} = v_c/i_n = [v_a + (v_3/m)]/i_a \tag{22}$$

$$v_a = i_a R_s;\ v_b = i_b R_L \tag{23}$$

$$i_b = [(m+n+1)/m]i_a \quad (24)$$

Hence:

$$R_{ae} = R_s + [(m+n+1)/m^2]R_L \quad (25)$$

But comparing equation (12) with equation (25) shows that

$$R_{ae} = 2R_s \quad (26)$$

In summary for two-way impedance match the following relationships occur:

Turns Ratio:	$n = m^2 (R_s/R_L) - m - 1$	(13)
Forward Gain:	$G = m^2 (R_s/R_L)$	(17)
Reverse Gain:	$G_r = 1/G$	(19)
Collector Load Impedance:	$R_{Lc} = (n+m) R_s$	(21)
Emitter Source Impedance:	$R_{se} = 2R_s$	(26)

Referring to FIG. **5**, there is shown a schematic circuit diagram of a preferred embodiment of the invention showing typical parameter values. The same reference symbols identify corresponding elements throughout the drawing. FIG. **5** includes an input coupling capacitor **22**, an output coupling capacitor **23**, an emitter biasing resistor **24** in series with an *r-f* choke **25**, biasing resistors **26** and **27**, bypass capacitors **31** and **32** and B+ terminal **33**. The circuit dissipates negligible *r-f* power. Resistors **24**, **26** and **27** do not dissipate *r-f* power because negligible *r-f* current flows through them. Were transformer **T1** and transistor **Q1** ideal and lossless, there would be essentially no *r-f* power loss between input and output. Because of the nature of the circuit, the circuit dynamic range corresponds substantially to that of transistor **Q1**.

With the circuit of FIG. **5** and **10** ma. delivered into terminal **33** at 15 volts, the invention had a gain of 8dB± 0.25 dB from 5 to 350 MHz. For input and output impedance of 50 ohms the maximum VSWR was 1.5 from 5 to 100 MHz and 2 from 100 to 250 MHz. The maximum noise figure was 1.2 dB from 5 to 150 MHz and 1.5 dB from 150 to 200 MHz. The minimum power output at 1dB compression over 5 to 150 MHz was 10 dBm and from 150 to 200 MHz **9** dBm.

There has been described a novel *r-f* amplifying circuit characterized by matching source and load impedances and good amplification over a relatively broad bandwidth while using relatively few components, components that need not be adjusted and are relatively economical. It is evident that those skilled in the art may now make numerous uses and modifications of and departures from the specific embodiments described herein without departing from the inventive concepts. Consequently, the invention is to be construed as embracing each and every novel feature and novel combination of features present in or possessed by the apparatus and techniques herein disclosed and limited solely by the spirit and scope of the appended claims.

What is claimed is:

1. Amplifying apparatus comprising,
amplifying means having at least control, input and output electrodes,
a common terminal,
transformer means having at least a primary and a secondary winding,
said secondary winding having a tap intermediate to first and second portions thereof,
an input terminal,
an output terminal,
means for coupling said output terminal to said tap,
means for coupling said primary winding between said input terminal and said input electrode,
said first portion being coupled between said tap and said common terminal,
said second portion being coupled between said tap and said output electrode,
and means for coupling said control electrode to said common terminal.

2. Amplifying apparatus in accordance with claim **1** wherein the turns ratio between said first portion and said primary winding is m and between said second portion and said primary winding is n with $n = m^2 R_s/R_L - m - 1$ wherein R_s is a predetermined source resistance and R_L is a predetermined load resistance.

3. Amplifying apparatus in accordance with claim **2** and further comprising said source resistance coupled between said input terminal and said common terminal and said load resistance coupled between said output terminal and said common terminal.

4. Amplifying apparatus in accordance with claim **1** wherein said amplifying means comprises a transistor and said control, input and output electrodes comprise base, emitter and collector electrodes, respectively.

5. Amplifying apparatus in accordance with claim **4** and further comprising,
a source of d-c operating potential connected to said collector electrode through said secondary winding,
and means for biasing said base and emitter electrodes.

6. Amplifying apparatus in accordance with claim **5** wherein the means for biasing said base electrode comprises a first resistor connected between said source of d-c potential and said base electrode and a second resistor connected between said base electrode and said common terminal and the means for coupling said base electrode to said common terminal comprises an *r-f* bypass capacitor and further comprising,
another *r-f* bypass capacitor coupling said source of a d-c potential to said common terminal.

7. Amplifying apparatus in accordance with claim **6** wherein said means for biasing said emitter electrode comprises an emitter biasing resistor in series with an *r-f* choke between said common terminal and said primary winding.

8. Amplifying apparatus in accordance with claim **7** wherein said means for coupling said primary winding between said input terminal and said emitter electrode comprises a capacitor and said means for coupling said output terminal to said tap comprises a capacitor.

* * * * *

Appendix E Manual Backdating

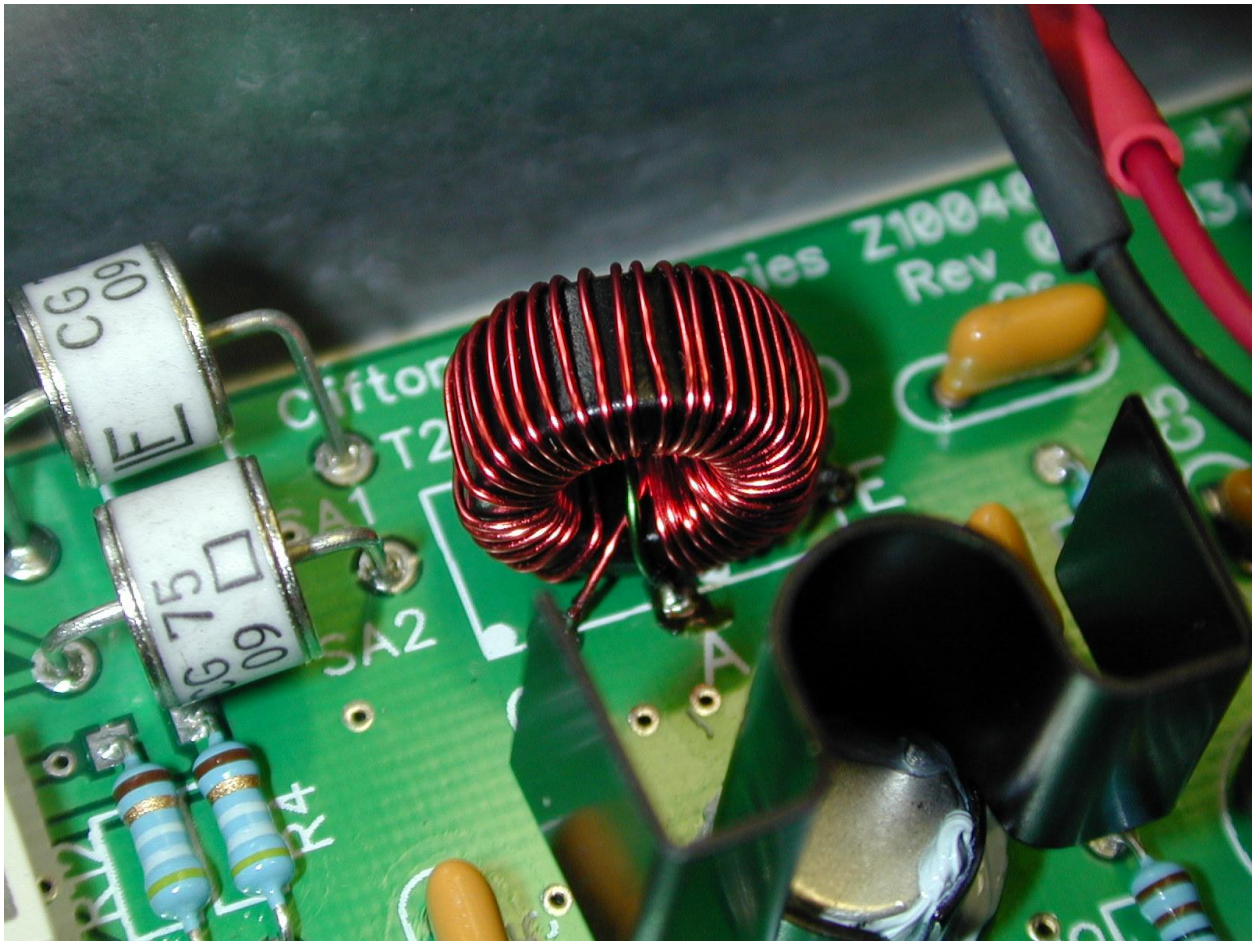
There are no manual backdating pages.

Appendix F Z10042A Performance Increased Gain

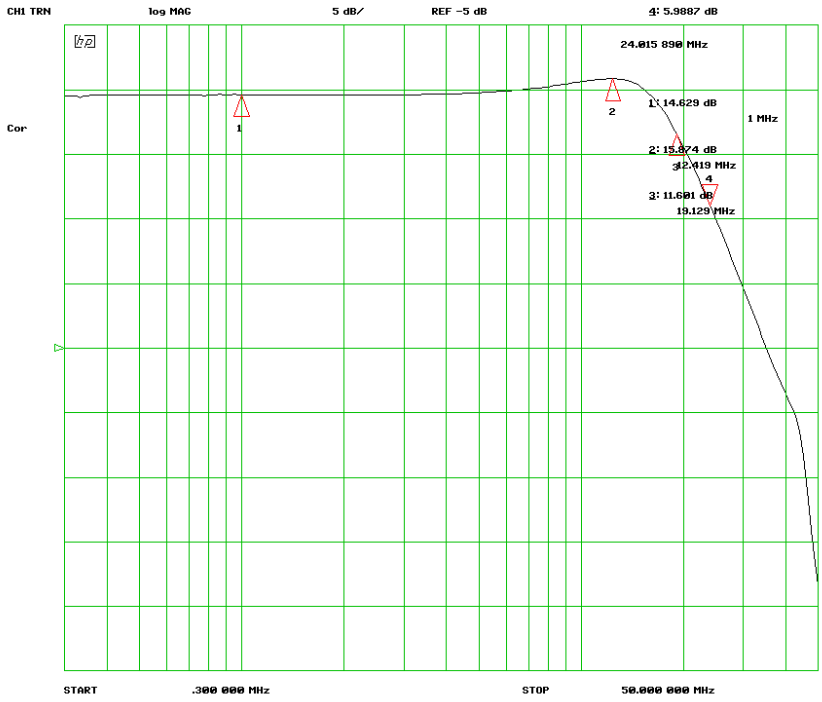
This appendix describes the expected performance changes when a Z10042A is built with a 1:29:6 turns ratio. The data provided is from a sample of one Z10040B amplifier and while believed accurate, some unit-to-unit variation may be expected. The Z10042A will have similar performance vis-à-vis T2 and T4 transformer turns, so it safe to extrapolate performance from the through hole, series feed Z10040B to the shunt fed, surface mount Z10042A amplifier. It is likely, however, that the Z10042A will have better low frequency response with 1:29:6 turns than the sample Z10040B amplifier.

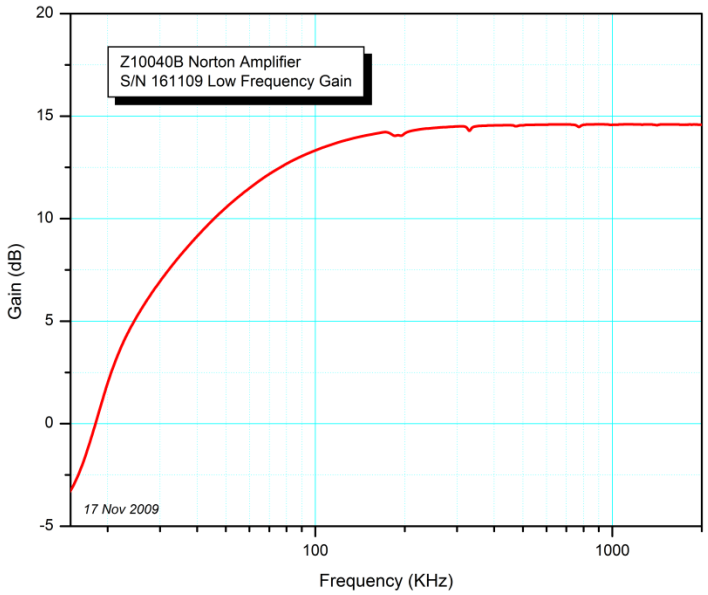
As discussed earlier in this manual, a Norton amplifier's gain is defined by the transformer (T2 and T4) turns ratio, with the "normal" Z10042A being constructed with a 1:11:4 turns ratio. From the Norton patent, the theoretical gain when built with a 1:29:6 turns ratio is $20*\log_{10}(6)$ or 15.6 dB. In practice, a dB or so loss from theoretical gain should be added to reflect losses in the input and output transformers among other sources.

The illustration below shows T2 built with a 1:29:6 turns ratio. #24 AWG wire can be used, but as the photo shows, it's a tight fit.



As might be expected, increased gain comes at a price; the upper -3 dB point is significantly below the 1:11:4 standard Z10042A amplifier. The figure below shows 14.6 dB gain at 1 MHz, with the upper -3 dB point being 19.1 MHz. (The standard 1:11:4 Z10042A has an upper -3 dB point around 40 MHz.) The lower -3 dB point is 65 KHz, essentially unchanged from the standard 1:11:4 amplifier.





With respect to other key performance measures, the 1:29:6 version shows:

- 3rd order intermodulation intercept (output referenced) degrades to +32 dBm
- 2nd order intermodulation intercept (output referenced) degrades to approx. +90 dBm
- Noise figure is not materially different from the 1:11:4 version.